TECCIENCIA

Development board based on the TMS320F28335 DSP for applications of power electronics

Placa de desarrollo basado en TMS320F28335 DSP para aplicaciones de electrónica de potencia

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Abstract

This paper presents the design of a special purpose development board for power applications based on the digital signal processor (DSP) TMS320F28335. We also propose some considerations for the design of any four-layer printed circuit line with international recommendations to counteract the EMI (electromagnetic interference) and increase the EMC (electromagnetic compatibility). Additionally, the main features of each module on the board and their respective conditioning circuits designed are presented in order for the development board to be useful for any application of power electronics as motor control, switching power supplies, LED lighting, communications through the electric network, etc. Finally, a test protocol to verify the performance of the card and the comparison between the final cost per unit and similar cards on the market were performed.

Key Words: anti-aliasing filter, electromagnetic interference, multilayer printed circuit board, signal conditioning, sensitivity.

Resumen

En el presente artículo se presenta el diseño de una tarjeta de desarrollo de propósito específico en aplicaciones de potencia con base en el procesador digital de señales (DSP) TMS320F28335. Se proponen además unas consideraciones para el diseño de cualquier circuito impreso de cuatro capas acordes con las recomendaciones internacionales para contrarrestar los efectos de interferencia electromagnética (EMI) y aumentar la compatibilidad electromagnética (EMC). Como factor adicional se presentan las principales características de cada modulo en la placa y sus respetivos circuitos de acondicionamiento, esto con el fin de que la placa de desarrollo sea útil para cualquier aplicación de electrónica potencia como control de motores, fuentes conmutadas, iluminación LED, comunicaciones a través de la red eléctrica, etc. A continuación, se realizó un protocolo de pruebas para verificar el funcionamiento de la tarjeta y la comparación entre el costo final por unidad y las tarjetas similares presentes en el mercado. Finalmente, se presentan las conclusiones en donde se resalta que la tarjeta implementada cumple con las características adecuadas para operar en el desarrollo de prototipos electrónicos de potencia a nivel de innovación y/o investigación.

Palabras clave: Acondicionamiento de señales, circuito impreso multicapa, filtros antialiasing, interferencias electromagnéticas, sensibilidad.

1. Introduction

Today, renewable energies have gained a lot of importance in the sustainable development of nations. Worldwide energy consumption of renewable sources exceeds 25% and is expected to increase by 50% at the middle of this century. Societies are increasingly consuming such resources in order to achieve energy coverage for the entire population. The wide array of renewable energy sources includes solar, wind, geothermal, biomass, tidal, and wave power, among others [1].

Thus, the Investigation Group LIFAE (the Spanish acronym for Research Laboratory of Alternative Sources of Energy) of the Universidad Distrital Francisco José de

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Caldas in Bogotá, Colombia investigates such issues, specifically photovoltaic systems, solar radiation and ambient temperature characterization, stand-alone and interconnected systems, and their respective applications. These investigations have been based on energy processing, understood as the transformation of renewable energies into electricity suitable for isolated loads or grid feeding and associated power electronics (topologies of DC-to-DC converters, inverters, Voltage-Source Converters (VSC) and High-Voltage Direct Current (HVDC) based on VSC) [2].

To accomplish the above, computer systems with high processing capabilities are required in order to properly develop control algorithms and perform energy management. Hence, the need arises for low-cost devices which operate at high frequencies, have low consumption, the capacity for signal processing in real time, a high level of integration, high resolution and are adaptable to specific applications of power electronics, which perform the processing of energy [3].

Consequently, in this study we seek to analyze a purpose board specific for applications in power electronics in order to support the DSP, which is an electronic device that fully meets the above characteristics. Furthermore, we expect the development of a series of circuits which allow for peripherals to adapt to the function required, as well as the adaptation of analog to digital signals, the modification of the Pulse-Width Modulators (PWM), the conditioning of general-purpose input/output signals, and the implementation and operation of different communication systems (I2C, SPI, etc.) for the transmission of signals of interest such as the signals transmitted to the Digital-to-Analog Converter (DAC), among others.

2. Methods and materials

2.1. DSP Selection

The wide variety of specialized digital signal processors in different electric and electronic applications, require taking into account specific criteria for the selection of DSP, such as arithmetic format, data bus, speed of execution and transmission, memory size, number of PWM channels, sample rate and resolution of the analog-to-digital converter. Thus, the selection of specific DSP provides adequate performance to the system in which the processor is going to be included [4].

The DSP was selected considering it would have a floating-point format. It is ideal for applications requiring flexibility, high dynamic range and accuracy. A second parameter that was considered was the operation frequency. In addition, the amount and variety of peripherals were also taken into account. In this way, and based on the above, it was established that the Texas Instrument processor TMS320F28335 was the processor which meets the criteria at an appropriate cost.

2.2. Digital Signal Processor TMS320F28335

The TMS320F28335 is a 32-bit floating-point DSP belonging to the sub-family of Texas Instruments C2000 Delfino, which combines the versatility of a general-purpose microcontroller with the high precision and performance of a digital signal processor. It is made of technology CMOS, can operate at a frequency of 150 MHz and has modified Harvard architecture. From a power electronics perspective, the most important module is the pulse width modulation. There are six of these modules, where each consists of two complementary outputs containing a common 16-bit counter. Each time a sample parallel is taken, a channel of each module can work at a higher resolution (24 bits).

Furthermore, the DPS has 16 channels for analog-to-digital converter module with 12-bit resolution at a fast conversion speed up to 80 ns. The improved quadrature encoder module is considerably useful for obtaining information on the position, direction and speed of a rotary machine. It has three 32-bit timers and has a varied group of protocols in the communication port [5]: Serial Peripheral Interface (SPI), Inter-Integrated Circuit (IIC), Controller area Network (CAN), Serial Communication Interface (SCI).

2.3. Modules adapted to the development board

The development board is divided into four groups, as shown in **Figure 1.** In the ADC module there are circuits with analog signals and it consists of anti-aliasing filters, conditioners, circuits of protection and overvoltage, and analog-to-digital converter (ADC). The module named in the figure as "PWM, QUEP. CAP, GPIO" goes to the digital part consisting of PWM generator, module of capture external events (CAP), incremental rotary encoder interface (QEP) and module to the General-Purpose Input/Output signals (GPIO). Similarly, the module appearing as "SPI, CAN, SCI, IIC" consists of the communication port conformed by the modules (SPI, IIC, SCI, CAN). In addition, there is a DAC module and a module including the polarization sources for both the digital part and analog part.
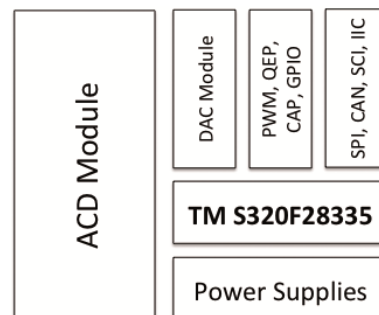

Figure 1 Physical distribution of the modules on the development board.

The signal generator module PWM has 12 independent channels. Signal conditioning was implemented through the level shifter CD4504b IC (Integrated Circuit), which allows for three (3) different output voltage values (3.3, 5, 15) V. It includes four (4) buttons for handling external interrupts, which are responsible for forcing the output level of the PWM signal to a level predefined by software. The GPIO module was conditioning by the IC of the 74LVC245ADWR bidirectional data Buffer. This module has 27 shared inputs/outputs and six (6) independent inputs/outputs with the output voltage level conditioned as the PWM module, as shown in **Figure 2**

The eCap is exclusively dedicated to the accurate capture of external events. It presents six (6) channels that can perform as an auxiliary PWM signal generator.

The eOEP module was likewise adapted as an interface between an incremental rotary encoder and the DSP. It has a Quadrature Decoder Unit (QDU), a Position Counter and Control Unit (PCCU) and a Unit time base for speed/frequency Measurement (UTIME).

Because the DSP does not have an analog-to-digital converter, the SPI for the exchange of data between the DAC and the DSP was defined, since it offers a higher transmission speed than the IIC and the tuple data is 16 bits. **Figure 3** shows the electric circuit implemented for such convertor. DAC module has a 12-bit resolution channel and an output signal between (3-0) V, conditioned to the board by the IC MCP 4921.
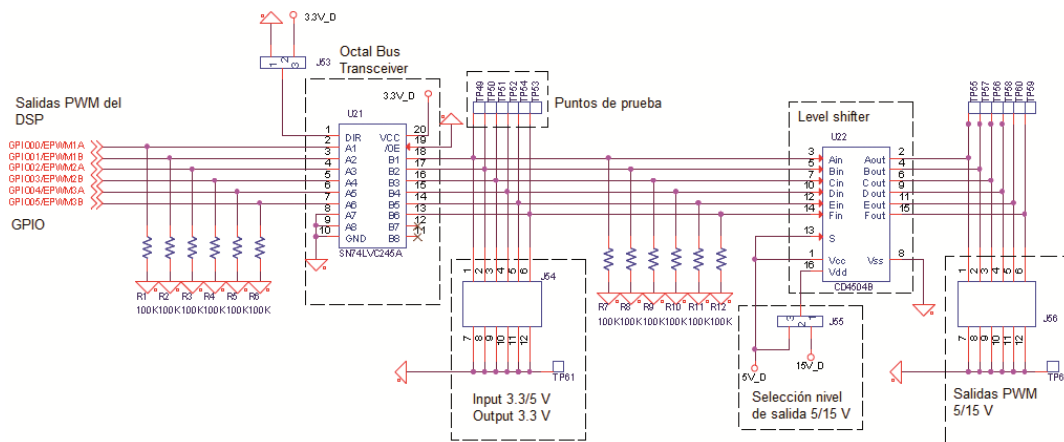
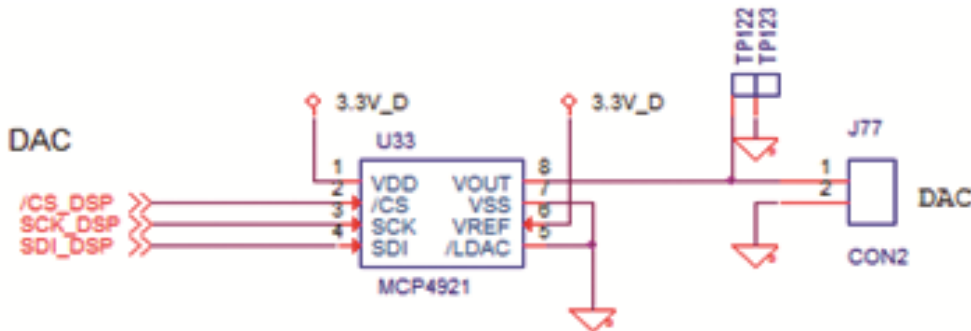

Figure 2 Conditioning of the PWM and GPIO signals

Figure 3 Electric circuit implemented for the DAC.
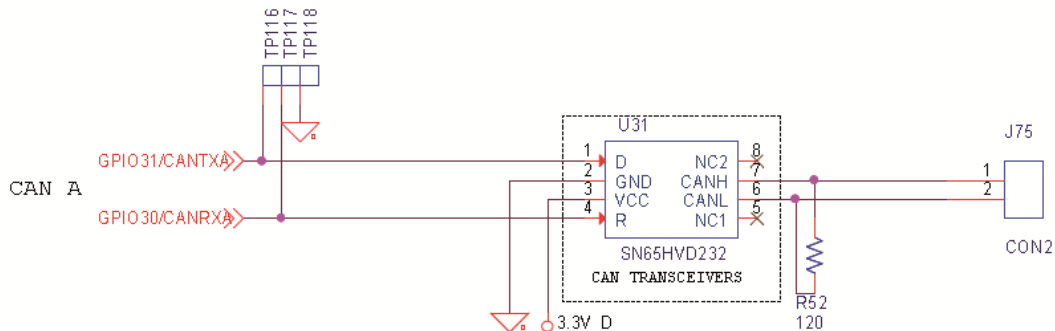

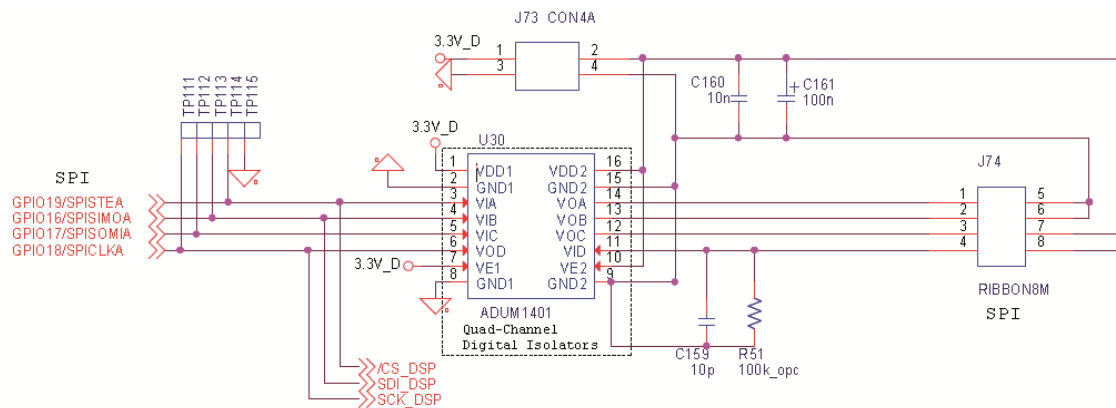**Figure 4** Adaptation Circuit of the Common Protocol - CAN.

Figure 5 Conditioning of the SPI standard.

The CAN protocol is based on the Carrier Sense Multiple Access model with a transmission rate up to 1 Mbps and a range of 40m. It discerns between temporary errors and permanent failures of nodes. It is adapted to the ISO 11898 Standard by the IC SN65HVD232 *CAN transceiver,* as shown in **Figure 4**

The SCI is an asynchronous serial communication protocol with double buffer for transmission and reception functions. It is adapted to IC SN75179B *differential driver and receiver pair*, and is ideal for applications with balanced transmission lines in the RS-485 and RS-422 standards.

The ICC Module has a transmission rate of between 10 kbps and 400 kbps. It is compatible with the Semiconductors IIC-bus v2.1 and is decoupled through the IC ADuM1250.

The conditioning of the peripheral SPI was performed through the integrated circuit ADuM1401 of four separate and isolated channels, which are based on Analog Devices, Inc., iCoupler® technology, as seen in **Figure 5.**

This device is characterized by its low power consumption (a tenth of the conventional optocouplers, approximately) and ease of operation. It was created to be used in applications with SPI interface for converting data with a transmission rate up to 90 Mbps.

2.4. Anti-aliasing filter - ADC Module

Signals acquisition was made by the analog-to-digital converter, which performs a sampling that must satisfy the condition of the Nyquist–Shannon sampling theorem. In case this parameter fails to be met, a phenomenon known as Anti-aliasing occurs [6]. Therefore, by means of a low-pass filter, any signal outside the range of interest (sampled signal) gets eliminated and the presence of such phenomenon avoided.

Topology selection focused on the searching of the one involving less active elements, thereby decreasing the cost

of the filters and the space on the printed circuit board (PCB).

Of the main topologies [7] [8], Sallen-Key Topology (**Figure 6 a**) and Multi FeedBack (MFB) Topology (**Figure 6 b**) both contain a single operational amplifier for a second order filter. Among these two, a sensitivity analysis was performed [7], defined in Equation 1 where *y* represents parameters that mathematically model the filter and *x* represents the values of resistors and capacitors conforming the filter, thus finding the topology representing less percentage changes in the quality factor Q and in the natural frequency of the filter ω_0, according to the percentage changes in the market values of the passive elements composing it. Topology to be selected was based on the sensitivity calculations, the resistance for frequencies and the lower value of the synthesis of the sensitivities.

$$S_x^y = \frac{\partial y}{\partial x}\frac{x}{y} \quad (1)$$

2.5. PCB Design

Currently available technology has led to have circuits with a higher level of integration, considerably reducing the sizes of the PCB and thus increasing the capacity of interfering one signal into another and, in general, adverse electrical factors affecting signal integrity.
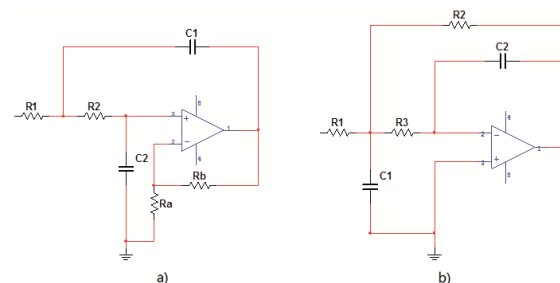

Figure 6 (a) Sallen-Key Topology, (b) Multi FeedBack Topology

PCB design for the implementation of the board and in general for any multilayer PCB, was based on the following considerations so that the effects of EMI and EMC counteract [9] [10] [11] [12] [13] [14]:

- The outward and return path of a signal should be close enough so that the inductance of the circuit is reduced and thus the magnetic field flux generated.

- The larger the area of the conductor is the reactance substantially decreases, thus controlling the effects of electric and magnetic fields.

- Creating return planes on the signal layer helps to substantially lower the inductance of the paths and therefore the total inductance of the PCB. This plane catches and drains the radiation generated by the signals interacting in the printed circuit board

- If the PCB presents return planes in the outer layers, must be verified that there are not small isolated copper areas (*island*) as these behave likely as microstrip antennas, susceptible to radiate electromagnetic fields of adjacent signals. Moreover, if there are large copper segments that are not connected to the ground plane on the return plane, these must be grounded via routes known as *"stitching vias"*.

- Linear polarization and analog and digital ground planes must be separated, as shown in **Figure 7**.

- Location of the parts having connections in common should be as close as possible and the copper traces short and straight. In digital circuits, if the above condition cannot be met, parts that are functionally related must kept close or the pieces with clock signals at high frequencies and very short rising edges must be grouped. Thus, the size of the paths carrying these signals can be minimized.

- In accordance with the IPC 2251, paths greater than $\lambda/15$ length, must be designed according to the transmission lines theory.

- In mixed PBC, meaning those composed of analog, digital and power circuits, these must be distributed in different areas and only if necessary, join them into a single point. If along the PCB different frequency bands are presented, components whose signals have low spectral components should be located inside the plate. Moreover, components with higher frequency signals must be located in the periphery of the PCB, previous to the connectors.

- Likewise, the following parameter for the distribution layers was considered: signal layers must be as close as possible to ground planes in order for EMI to reduce.

- Linear polarization must be adjacent to ground/return planes for adding capacitances between planes, which helps to reduce polarization noise and electromagnetic radiation.

For the separation of copper paths, the 3W Rule is suggested, which states the spacing distance as three times the width of the path, between traces centers.

- Avoid 90 degrees angles on paths carrying signals in high frequency band or higher, as these increases the width of the track with a factor of 1.414, thus affecting the characteristic impedance at the corners of the paths. Thereby, changes in the trajectory greater than 45 degrees are not recommended.

- The use of decoupling capacitors helps filtrating the radiofrequency noise present in the signal power of integrated circuits. To use two or three different types of capacitors (tantalum, ceramic, electrolytic, etc.) with values decline for decades from 0.1 nF is recommended.
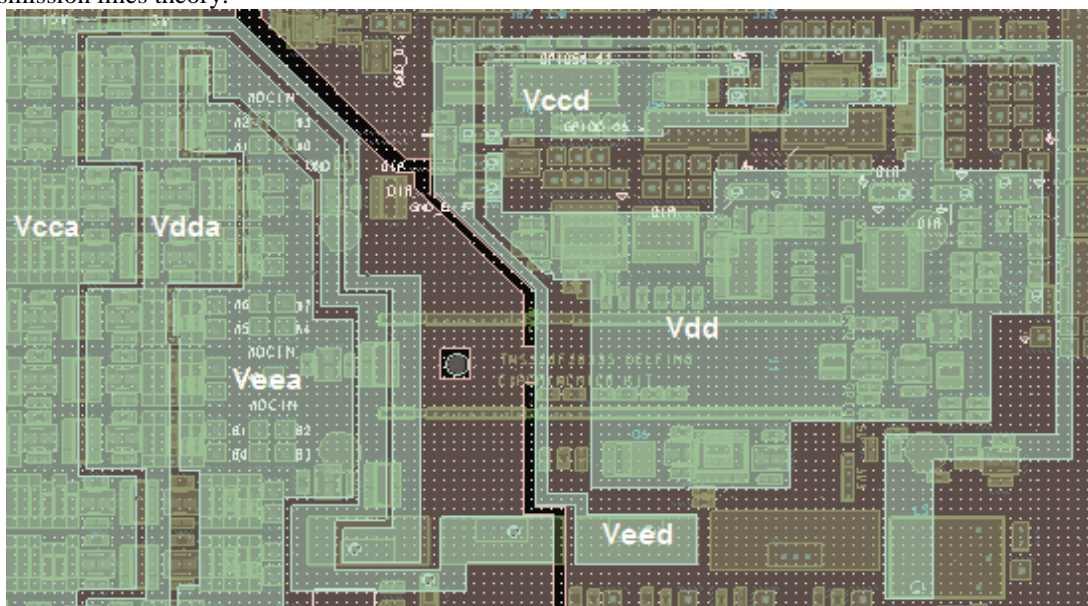
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Figure 7 Separation of linear polarization and analog and digital ground planes.

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3. Results

3.1. Topology definition for the antialiasing filter

In accordance with the procedure described in section 2.4, sensitivities shown in **Table 1** (were recommendation [9] was also followed to decrease sensitivity in the Sallen-Key topology regarding passive elements), were obtained. The statements in this table are given by the combination of the nominal values of the passive elements, which in turn, are in function of the frequency response required to implement. Such response is established towards minimizing the distortion in phase and magnitude to the signals to be sampled [16] [17] [18] [19]

For such reason, frequency response of the Bessel type was selected, whose transfer function for a second order

filter is given by (2) and whose denominator is a second degree Bessel polynomial [20]. By matching this with the transfer functions of the topologies, statements contained in **Table 2** are generated.

$$\frac{3\omega_c^2}{s^2 + 3s\omega_c + 3\omega_c^2} \tag{2}$$

By replacing equations of **Table 2** in the statements of **Table 1**, in **Figure 8** are presented the behaviors for the Sallen-Key topology, whose sensitivities are independent of f_c, and in **Figure 9** the behaviors shown for the MFB topology, taking into account different orders of magnitude of the product $C_1 f_c$. (f_c is the cut-off frequency of the filter).

Table 1 Sensitivities Calculation.

S_x^y	Sallen-Key Topology	Multi feed back Topology
$S_{C_1}^Q = \frac{dQ}{dC_1} * \frac{C_1}{Q}$	$1/2$	$1/2$
$S_{C_2}^Q = \frac{dQ}{dC_2} * \frac{C_2}{Q}$	$-1/2$	$-1/2$
$S_{R_1}^Q = \frac{dQ}{dR_1} * \frac{R_1}{Q}$	$\frac{R_2 - R_1}{2(R_1 + R_2)}$	$\frac{\sqrt{\frac{R_2 R_3}{R_1}}}{4\left[\sqrt{\frac{R_2 R_3}{R_1}} + \sqrt{\frac{R_2}{R_3}} + \sqrt{\frac{R_3}{R_2}}\right]}$
$S_{R_2}^Q = \frac{dQ}{dR_2} * \frac{R_2}{Q}$	$\frac{R_1 - R_2}{2(R_1 + R_2)}$	$\frac{2R_1 R_2 R_3 \frac{R_2}{\sqrt{R_1}} + R_1\left(R_2{}^2 - R_3{}^2\right) + R_2{}^2 R_3{}^2}{4R_1 R_2 R_3 \left[\sqrt{\frac{R_2 R_3}{R_1}} + \sqrt{\frac{R_2}{R_3}} + \sqrt{\frac{R_3}{R_2}}\right]^2}$
$S_{R_3}^Q = \frac{dQ}{dR_3} * \frac{R_3}{Q}$		$\frac{2R_1 R_2 R_3 \frac{R_3}{\sqrt{R_1}} + R_1\left(R_3{}^2 - R_2{}^2\right) + R_2{}^2 R_3{}^2}{4R_1 R_2 R_3 \left[\sqrt{\frac{R_2 R_3}{R_1}} + \sqrt{\frac{R_2}{R_3}} + \sqrt{\frac{R_3}{R_2}}\right]^2}$
$S_k^Q = \frac{dQ}{dk} * \frac{k}{Q}$	$\frac{C_1 R_1}{C_2(R_1 + R_2)}$	
$S_{C_1}^{\omega_0} = \frac{d\omega_0}{dC_1} * \frac{C_1}{\omega_0}$	$-\frac{1}{2}$	$-\frac{1}{2}$
$S_{C_2}^{\omega_0} = \frac{d\omega_0}{dC_2} * \frac{C_2}{\omega_0}$	$-\frac{1}{2}$	$-\frac{1}{2}$
$S_{R_1}^{\omega_0} = \frac{d\omega_0}{dR_1} * \frac{R_1}{\omega_0}$	$-\frac{1}{2}$	0
$S_{R_2}^{\omega_0} = \frac{d\omega_0}{dR_2} * \frac{R_2}{\omega_0}$	$-\frac{1}{2}$	$-\frac{1}{2}$
$S_{R_3}^{\omega_0} = \frac{d\omega_0}{dR_3} * \frac{R_3}{\omega_0}$		$-\frac{1}{2}$
$S_k^{\omega_0} = \frac{d\omega_0}{dk} * \frac{k}{\omega_0}$	0	

Table 2 Resistance values for frequency response of the Bessel type.

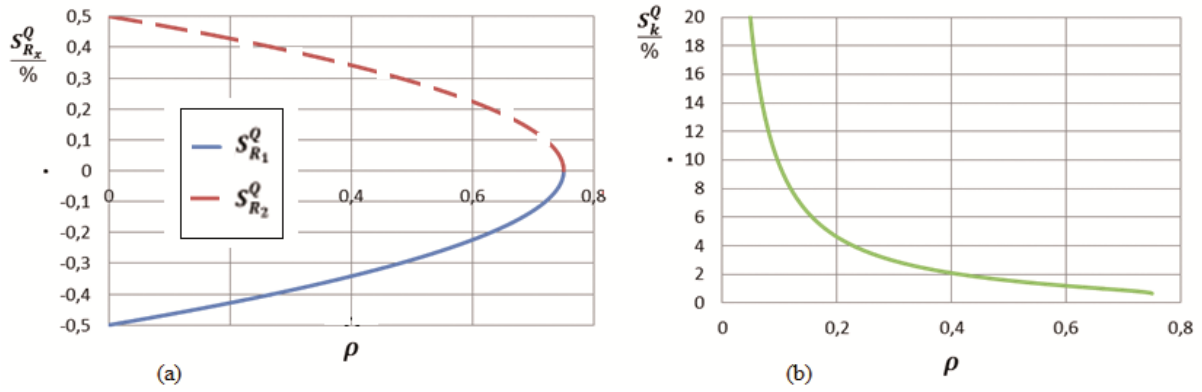| R_X	Sallen-Key Topology + Bessel	Multi FeedBack Topology
R_1	$R_1 = \frac{1}{\rho C_1 \omega}\left(\frac{\sqrt{3}}{6}\sqrt{3 - 4\rho} + \frac{1}{2}\right)$ $\rho = C_2/C_1$	$R_1 = R_2 = \frac{1}{\rho C_1 \omega}\left(\frac{\sqrt{3}}{6}\sqrt{3 - 8\rho} + \frac{1}{2}\right)$ $\rho = C_2/C_1$
R_2	$R_2 = \frac{1}{\rho C_1 \omega}\left(-\frac{\sqrt{3}}{6}\sqrt{3 - 4\rho} + \frac{1}{2}\right)$ $\rho = C_2/C_1$	$R_1 = R_2 = \frac{1}{\rho C_1 \omega}\left(\frac{\sqrt{3}}{6}\sqrt{3 - 8\rho} + \frac{1}{2}\right)$ $\rho = C_2/C_1$
R_3		$R_3 = \frac{1}{\rho C_1 \omega}\left(-\frac{\sqrt{3}}{12}\sqrt{3 - 8\rho} + \frac{1}{4}\right)$ $\rho = C_2/C_1$

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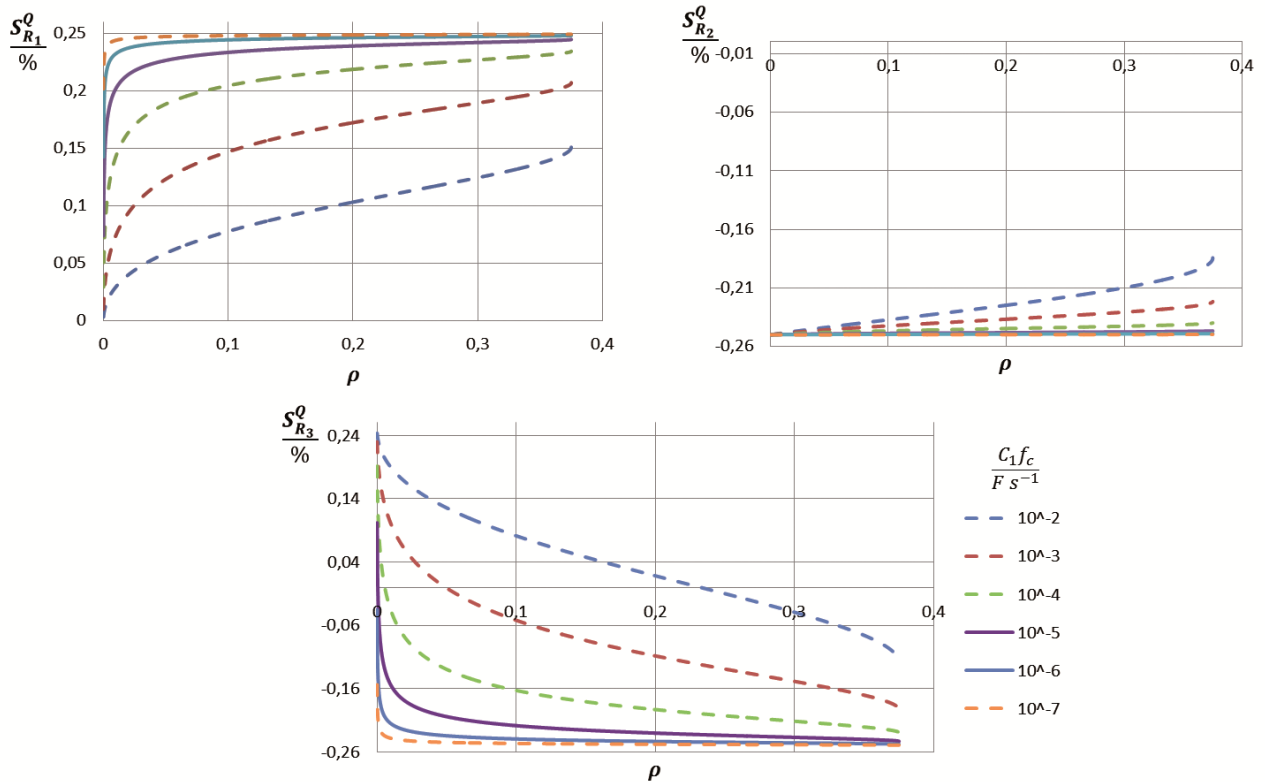Figure 8 $(a) S_{R_x}^Q$, $(b) S_k^Q$ Sallen-Key Topology

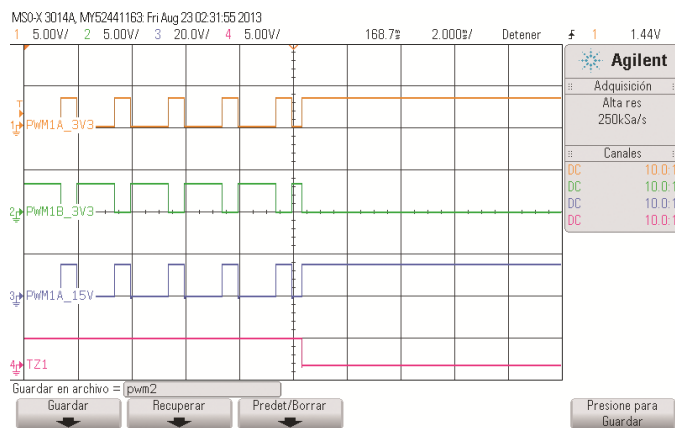Figure 9 $S_{R_1}^Q$, $S_{R_2}^Q$, $S_{R_3}^Q$ Multi FeedBack Topology.

Figure 10 Effect of external interrupt (TZ1) over the PWM1x channel.

3.2. Operating Tests

Figure 10 shows the behavior of the signals when pushing the button P1 (associated to TZ1), imposing a high level for PWM1A and a low level for PWM1B. These levels are predefined in the TZCTL configuration register associated to each PWMxx channel. On the other hand, resulting signal of the voltage booster was captured in channel 3 of the oscilloscope, which is responsible for increasing the amplitude up to 15 V.

Figure 11 shows the transmission of the word "hexadecimal 7555", along with a configuration mode of the clock signal (0,0), that is to say, the bit transmission is given by each rising edge without delay. MISO signal is captured in channel 1 of the oscilloscope for which the logic level at an idle state is high and a transmission rate of 300 kbps. Channels 2 and 3 respectively record SS and SCLK signals.
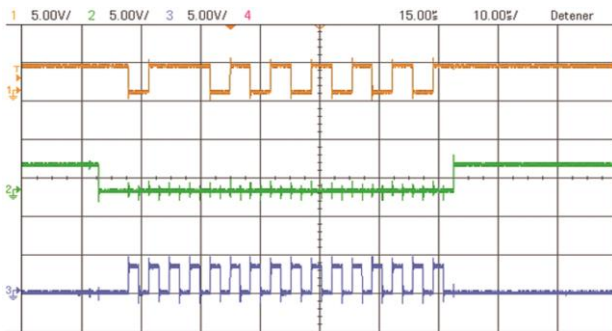

Figure 11 SPI Standard, configuration of the clock signal CPHASE =0, CPOL = 0.

On the third test the ADC module was used, in which a sinusoidal input signal to the filter entrance was introduced with a frequency corresponding to the cutoff frequency (600 Hz), with amplitude of 15 V (**Figure 12**, Ch1). Channel 2 has the output signal of the filter with amplitude 10 V. Subsequently, the test signal is attenuated 10% and elevated to a DC level of 1.5 V, effectively obtaining a signal amplitude of 1V and 1.5V above the reference of channel 3 (Ch3). Finally, the test signal is digitized at a sampling rate of 735.3 ksps and transmitted to the DAC module for its conversion to analog (channel 4, Ch4).
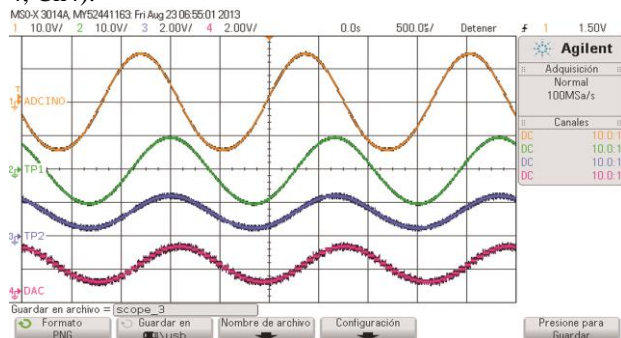

Figure 12 ADCIN0 Block -Filter- Conditioner- DAC

3.3 Comparison with similar boards commercially available

Although on the market there is a variety of development kits, evaluation boards and prototypes training, these are designed for general purpose applications, thus limiting the scope that can be achieved, since they include peripherals that are not specific for power electronics applications, taking up space on the PBC which can be used for conditioning or addition of related modules.

Table 3 shows those commercially available boards, similar to the ones developed in this project. Even though these are specific boards, do not include conditioning of their peripherals such as: different voltage levels for the PWM signals and specific purpose inputs/outputs, anti-aliasing filters and signal conditioning for the ADC module. Another factor to consider is the cost per unit, due to the 50% decrease compared with the cheapest board registered on **Table 3.**

Table 3 Comparison of the most representative similar boards on the market.

BOARD	MAIN FEATURES	COST PER UNIT
TI28335DSK-II	Based on the TMS320F28335 DSP, is specifically designed for industrial automation. Includes LCD, two communication terminals RS-232, SD card interface, switches for interrupting and Ethernet interface.	$ 950 000
ICETEK-F28335-A	Its main processor is the TMS320F28335 DSP. Includes 16 ADC channels for analog signals with width from -5 V to 5 V. 88 input/output of general purpose. Four (4) audio interfaces and two D/A0 converters.	$ 1 586 000
Motor Control Development for TMS320F28335 eZdsp™ with Socket	It provides hardware and software for motor control, software for using fuzzy logic and PID algorithms. It is built upon the TMS320F28335 processor.	$ 1 746 100

4. Conclusions

A development board for power electronics applications based on the Texas Instrument TMS320F28335 DSP, which meets the proper characteristics to developments of prototype and research was designed and implemented. It has the necessary circuitry for setting and conditioning of different modules associated to the DSP (PWM, DAC, ADC, SPI, I2C, CAN, SCI, eQEP, eCAP, GPIO) assembled on a PCB, which was designed based on recommendations made by international organizations and scientific articles published in the IEEE to counter the adverse effects of electromagnetic interference.

Acknowledgments

References

[1] Varun, R. Prakash y I. Krishnan Bhat, «Energy, economics and environmental impacts of renewable energy systems,» *Renewable and sustainable energy reviews,* vol. 13, nº 9, pp. 2716-2721, 2009.

[2] P. K. Steimer, «Enabled by high power electronics Energy efficency, renewables and smart grids,» de *Power Electronics Conference (IPEC), 2010 International*, Sapporo, 2010.

[3] Y. Huang, J. Li y R. Gong, «A novel SVPWM control Stand-alone Three-phase PV power system based on TMS320F28335,» de *Consumer Electronics, Communications and Networks (CECNet), 2012 2nd International Conference on*, Yichang, 2012.

[4] J. Salazar, «Procesadores digitales de señal (DSP),» *Mundo electronico,* nº 314, pp. 46-57, 200.

[5] Texas Instruments, «Data Manual: TMS320F28335, TMS320F28334, TMS320F28232, Digital signal controllers (DSCs),» Texas Instruments, 2007.

[6] P. Embree, C algorithms for real-time DSP, Prentice Hall, 1995.

[7] A. S. Sedra y K. C. Smith, Circuitos Microelectronicos, Oxford: Oxford University Press, 1999.

[8] H. G. dimopoulos, Analog Electronic Filters: theory, design amd synthesis, Springer, 2012.

[9] S. Muralikrishna y S. Sathyamurthy, «An overview of digital circuit design and PCB design guidelines - An EMC perspective,» de *Electromagnetic Interference & Compatibility, 2008. INCEMIC 2008. 10th International Conference on*, Bangalore, 2008.

[10] N. L. Eastman, «Considerations for mixed analog/digital PCB design,» de *WESCON/96*, Anaheim, 1996.

[11] J. Jing y K. Lingwen, «Study of signal integrity for PCB level,» de *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, Xi'an, 2010.

[12] J. López Sánchez, F. A. Rojas S., C. L. Trujillo y J. Guacaneme Moreno, «Recomendaciones para el diseño de circuitos impresos de potencia,» *Revista cientifica y tecnologica de la facultad de ingenieria universidad Distrital Francisco José de Caldas,* vol. 9, nº 2, pp. 44-47, 2003.

[13] See, «Impact of PCB Layout Design on Final Product's EMI Compliance,» de *17th International Zurich Symposium on Electromagnetic Compatibility*, Zurich, 2006.

[14] P. Chand, B. N. Gangopadhyay y M. Kumar, «PCB layout design for EMI/EMC compliance,» de *ElectroMagnetic Interference and Compatibility (INCEMIC), 2006 Proceedings of the 9th International Conference on*, Bangalore, 2006.

[15] W. Saraga, «Sensitivity of 2nd-order Sallen Key type active RC filters,» *Electronics letters,* vol. 3, nº 10, pp. 442-444, 1967.

[16] W.-. K. Chen, Passive, Active and digital filters, CRC Press, 2005.

[17] F. Miyara, Filttos Activos. E-book, Rosario: Universidad Nacional de rosario, 2004.

[18] P. Horowitz y W. Hill, The art of electronics- 2nd Edition, Cambrige University Press, 1989.

[19] M. Thompson, Intuitive Analog circuit design, 2nd Edition, Nownes, 2013.

[20] J. L. Dominguez Barragan, «Acondicionamiento de Mfilters,» Universidad de las americas Puebla , Puebla, 2003.

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