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SIMULATION OF A CMOS RFC OPERATION AMPLIFIER CIRCUIT WITH NEW RESULTS OF DC GAIN

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Seyed Vahid Feizbakhsh
Islamic Azad University,
Department of Electrical Electronics Engineering,
Mahabad Branch, Mahabad, Iran
avatvahidi@gmail.com

Ghader Yosefi
Islamic Azad University,
Department of Electrical Electronics Engineering,
Mahabad Branch, Mahabad, Iran
g.yosefi@iau-mahabad.ac.ir

Resumen: En este trabajo, volvemos a hacer la simulación de un reciclaje de cascode plegado (RFC) op-amp que fue publicado por Rida S. Assaad y et todos, en IEEE Journal of Solid-State Circuits. Los autores presentaron y simularon el circuito de RFC para obtener la ganancia de CC utilizando solamente análisis de AC. Alcanzaron los resultados que con el aumento del factor de k (la proporción de transistores del par cruzados en el circuito de RFC) la ganancia de CC se puede mejorar. Pero, criticamos su trabajo científicamente y presentamos un resultado contrario. Calculamos y analizamos la transconductancia y la resistencia de salida del amplificador op de RFC usando análisis de DC y AC. Por lo tanto, proponemos nuevos resultados y demostrar este hecho que con el aumento de k (1,5 <k <3), la ganancia DC se reducirá de 51,8dB a 45,9dB. Los resultados de la simulación se consiguen utilizando el software Hspise en tecnología estándar CMOS de 0,18 µm. Los resultados obtenidos muestran una buena coordinación entre el análisis DC y AC para demostrar nuestra afirmación.

Palabras clave: RFC Op-Amp, CMOS, ganancia DC, DC y AC análisis

Abstract: In this paper, we re-do simulation of a recycling folded cascode (RFC) op-amp which was published by Rida S. Assaad and et all, in IEEE Journal of Solid-State Circuits. The authors presented and simulated the RFC circuit to obtain DC gain using AC analysis only. They achieved to the results that with increasing the factor of k (the ratio of cross couple transistors in RFC circuit) the DC gain can be improved. But, we criticize their work scientifically and present a contrary result. We calculate and analyze the transconductance and output resistance of RFC op–amp using both DC and AC analysis. So we propose new results and prove this fact that with increasing k (1.5<k<3), the DC gain will be dropped from 51.8dB to 45.9dB. The simulation results are achieved using Hspise software in 0.18µm CMOS standard technology. Obtained results show a good coordination between DC and AC analysis to prove our claim.

Keywords: RFC Op-Amp, CMOS, DC gain, DC and AC analysis

Citar, estilo APA: Feizbakhsh, S., & Yosefi, G. (2017). Simulation of a cmos rfc operation amplifier circuit with new results of dc gain . Revista QUID (Special Issue), 1051-1054.

1. INTRODUCTION

There are some operation amplifiers (op-amp) such as two stage, folded cascode (FC), gain boosting and telescope forms. They have wide range of applications analog and digital circuits. Recently the FC op-amp with high gain and large signal sowing in the present and future is used as most common architecture.

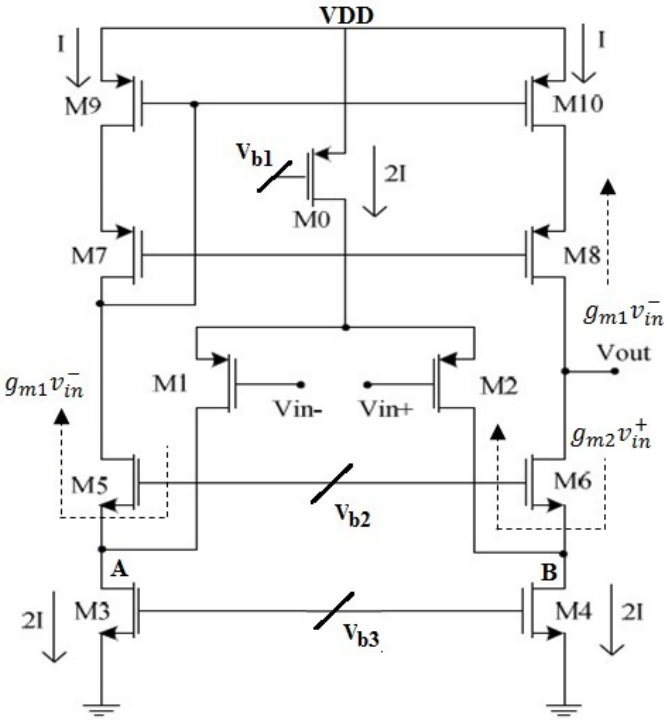
There are many authors (Assaad, 2009), (Valero,2015) which used multi methods to enhance the performance of the FC. The operational transconductance amplifier (OTA) is the important building block which they work on it to increase the DC gain and have a good phase margin (PM). For example, M. Mottghi (Kashtiban, 2006) changed the structure of cascode NMOS transistors to a simple current mirror for increasing amplifier's transconductance, Gm, and then to enhance DC gain. A. Dadashi 2011 changed the first stage of the FC and used the transconductance of the bulk of input MOS transistors to increase the total Gm. In The other work (Assaad, 2009) a cross couple was used in first stage as RFC op-amp to increase total Gm and then to have more DC gain.

In this paper we want to present re-analyzing and simulating RFC op-amp (Assaad, 2009) which had a basic problem in calculating DC gain. The authors only used AC analysis without paying attention to change DC bias current in the cascode transistors. So they declared that the DC gain can be enhanced with increasing the factor of k (the ratio cascode to cross couple transistors) and presented the advantages of RFC to FC op-amp only. They did not consider changing k along with changing DC bias current in RFC circuit.

Instead, we re-do necessary analysis and then simulate the RFC circuit using mathematical relations and Hspice software respectively. We will show that the increasing k (1.5<k<3) cause to droop DC gain from range of 80dB to 74dB and 51.8dB to 45.9dB with manual and simulation analysis respectively. In section 2, we consider the basic formulizations of transconductance in FC and RFC circuits. In section 3, we describe the DC analysis mathematically and form a table of numerical results. The AC analysis with simulation results and conclusions are also given in sections 4 and 5 respectively.

2. CONVENTIONAL FC AND RFC AMPLIFIER CIRCUITS

Before analyzing our work, let us consider the conventional FC and RFC op-amp circuits which are shown in Figures. 1 and 2. In this section we discuss on obtaining amplifier transconductances using injected currents to the outputs.



Figuire 1. Conventional Folded Cascode Operation Amplifier

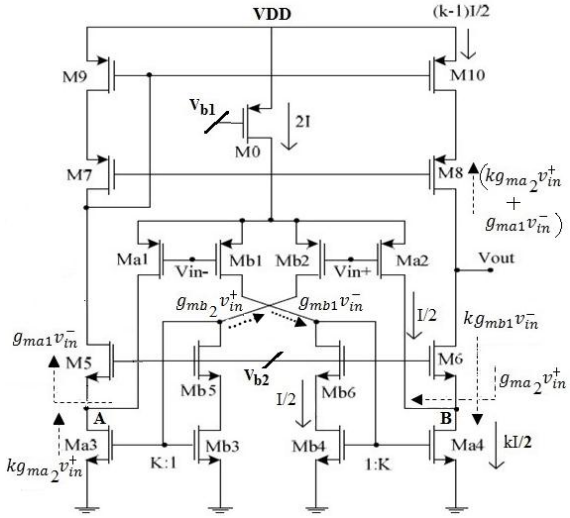


Figure 2. Conventional Recycling Folded Cascode Operation Amplifier [1]

3. SINGLE ENDED DC GAIN

According to Figure 1 we can write the relation of total amplifier transconductance, GmFC, as following equation:

$$G_{mFC} = g_{m1} \quad (1)$$

And the total AC injected current to the output node is:

$$i_{out} = g_{m1}v_{in}^{-} + g_{m2}v_{in}^{+} = 2g_{m1}\frac{v_{id}}{2} = g_{m1}v_{id} \quad (2)$$

Where $g_{m1} = g_{m2}$ and v_{id} is the voltage difference between v_{in}^{+} and v_{in}^{-}.

By taking into account $M_{1,2}$ (from Figure 1) is twice the size of M_{a1} (from Figure 2) and conducts double bias current of I, the transconductance of the RFC is demonstrated to be twice that of the FC (i.e., $g_{m1}=2g_{ma1}$). According to Fig. 2, the AC current of $g_{ma2}v_{in}^{+} + kg_{mb1}v_{in}^{-}$ (k is the size ratio of $M_{a3,4}$ to $M_{b3,4}$) is taken from the output node via M_6. Similarly the current $g_{ma1}v_{in}^{-} + kg_{mb2}v_{in}^{+}$ is also taken from he output node via left branch of current mirror (M_7 and M_9). Thus assuming $g_{ma2} = g_{ma1}$ and $v_{in}^{+} + v_{in}^{-} = v_{in}$, the total transconductanse G_{mRFC}, will be obtained as Equation (3):

$$i_{out} = g_{ma2}v_{in}^{+} + k \times g_{mb1}v_{in}^{-} + g_{ma1}v_{in}^{-} + k \times g_{mb2}v_{in}^{+} = g_{ma1}(1+k)v_{in}$$

$$\Rightarrow G_{mRFC} = g_{ma1}(1+k) \quad (3)$$

As we mentioned before, the authors R. S. Assaad and et all pointed that the increasing factor of k cause to enhance G_{mRFC} (Equation 3) and then to have more DC gain. In fact, the equation (3) expresses that the RFC has higher DC gain than the FC circuit. This is true but they used this relation with increasing k to have more DC gain without paying attention to this fact that the total output resistance, R_{out}, is reduced and cannot support their idea to have more DC gain in RFC circuit. This is because that the raising k changes DC bias current I in the cascode transistors of M_{a4}, M_6, M_8 and M_{10}. So in this case, R_{out} and then DC gain are reduced. We will prove this claim and present a contrary result of their work (Assaad, 2009) in the next sections.

4. Dc GAIN CONSIDERATIONS

According to Fig. 2, the transistors $M_{a1,2}$ and $M_{b1,2}$ have half size of M_0 (from Fig.1) and conduct bias current of I/2. The bias current of M_{b4} is mirrored in M_{a4} with amount of kI/2. Eventually with writing KCL in the node B, the bias current of M_6, M_8 and M_{10}, will be (k-1)I/2. Now let us consider the output resistance (R_{out}) and DC gain (A_v) relations, and calculate them numerically.

According to Fig. 2, in the right output of RFC circuit we have:

$$r_{o8} = \frac{1}{\lambda_p(k-1)I/2} \quad (4)$$

$$r_{o10} = \frac{1}{\lambda_p(k-1)I/2} \quad (5)$$

$$r_{o6} = \frac{1}{\lambda_n(k-1)I/2} \quad (6)$$

Before simulations, we calculate the equations of (4~13) using transistor sizes of table 1, bias current of I= 0.5 mA, V_{DD}=1.8v and changing k (1.5<k<3) numerically. The obtained results are given in table 2. According to it, we can see this fact that when the factor of k rises, the g_{m6} and g_{m8} are increased but r_{oa4}, r_{o6}, r_{o8} and r_{o10} are reduced and have more effect than the mentioned transconductance in R_{out}. As a result of this, the total R_{out} diminishes and causes to drop DC gain. These manual calculations are approximate and DC gain drops from 80dB to 74dB. However, we have a declining trend of Rout and DC gain.

Table 2. Numerical calculations of DC gain of RFC circuit (VDD=1.8v, I=0.5mA, λn= λp= 0.1)

	k=1.5			k=2			k=3		
	g_m (mA/v)	r_o (kΩ)	ΔV (v)	g_m (mA/v)	r_o (kΩ)	ΔV (v)	g_m (mA/v)	r_o (kΩ)	ΔV (v)
M_{10}	-	80	-	-	40	-	-	20	-
M_8	1.66	80	0.15	2.9	40	0.17	5	20	0.2
M_6	2.5	80	0.1	3.8	40	0.13	6.6	20	0.15
M_{a2}	1.66	40	0.3	1.66	40	0.3	1.66	40	0.3
M_{a4}	-	26.6	-	-	20	-	-	13.3	-
g_{mRFC}	4.16			5			6.66		
R_{out} (MΩ)	2.46			1.42			0.8		
A_v (dB)	80			77			74		

5. SIMULATION RESULTS

In the AC analysis, we simulated the RFC circuit with parameters of table 1 and using Hspice software in 0.18µm CMOS standard technology. The simulation results are shown in Fig. 3. It illustrates DC gain for FC and RFC op-amp circuits with amount of 29dB and 51.8~ 45.9dB respectively. As depicted in this figure, the DC gain of RFC circuit was improved and higher than the FC circuit.

These simulations are more accurate than manual analysis and it is observed that there is a declining trend of DC gain for RFC circuit with rising k (1.5<k<3).

Eventually, by comparing results of Fig. 3 and table 2, it is observed that there is a good coordination of declining trend of DC gain in the RFC circuit with rising k (1.5<k<3).

Fortunately in this case, the slew rate and noise analysis have no change and are the same result of reference (Assaad, 2009).

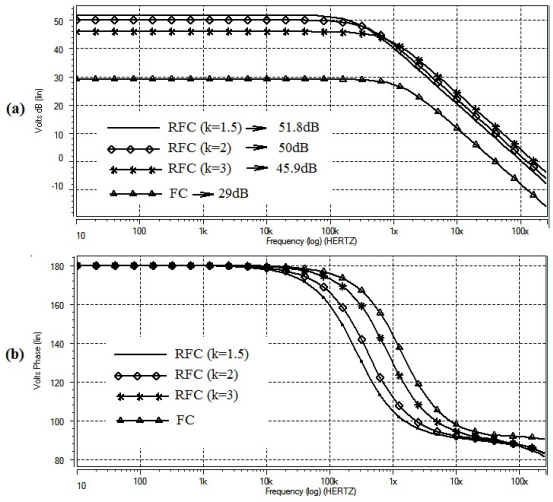


Figure *3. Simulation results of FC and RFC op-amp circuits: a) DC gain of FC is 29dB and for RFC is decreased from 51.8dB to 45.9dB with rising k (1.5<k<3). b) Phase Margin of FC and RFC circuits which is constant and about ~87* deg.

6. CONCLUSIONS

We re-analyzed and simulated the RFC op-amp circuit. In opposite of the conventional work, we proved that increasing factor of k (1.5<k<3) caused to decrease DC gain. For proving this claim, we calculated the transconductance, output resistance and then DC gain of RFC numerically. These manual calculations were approximate and DC gain dropped from 80dB to 74dB.
To have more accurate, the simulation results of RFC circuit were done using Hspice software in 0.18µm CMOS standard technology. In this case the obtained DC gain was decreased from 51.8dB to 45.9dB with rising factor of k (1.5<k<3). It was observed from manual and simulation analysis that there was a good coordination of declining trend of DC gain in the RFC circuit with rising factor of k (1.5<k<3).

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