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TITULO: CONFIGURATION OF THE OPERATION MODES FOR A SCINTILLATING FIBER SUB-DETECTOR IN LHCb

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CONFIGURACIÓN DE LOS MODOS DE OPERACIÓN PARA UN SUB-DETECTOR DE FIBRAS CENTELLEANTES EN EL EXPERIMENTO LHCb

CONFIGURATION OF THE OPERATION MODES FOR A SCINTILLATING FIBER SUB-DETECTOR IN LHCb EXPERIMENT

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ABSTRACT

The data acquisition boards will take advantage of the LHCb upgrade in the period between 2018 and 2019, during the Long Shutdown 2 of CERN experiments. These improvements aim to the configuration and re-structure of the data acquisition techniques, regarding the increase of the luminosity and its current collision center-of-mass energy. As such, the current condition of the detector, its acquisition techniques and protocols are documented. It will emphasize the Scintillating Fibers detector (SciFi), one of LHCb's future sub-detector in charge of trace pattern recognition by recording significant events in the data transmission. This paper shows a step-by-step presentation of the modifications applied to the codes, to move from a Standard Mode to a Wide Bus Mode, increasing the data rate by means of the reduction of the control bits. This improvement will enlarge the amount of analyzable information among the events.

Keywords: scintillating fibers; particle detectors; LHCb; VHDL programming; code configuration.

RESUMEN

Las tarjetas de adquisición se servirán de la actualización del LHCb, que tendrá lugar en el periodo entre 2018 y 2019, durante el Long Shutdown 2 de los experimentos del CERN. Estas mejoras apuntan a la configuración y re-estructuración de las técnicas de adquisición de datos, debido al incremento en la luminosidad y correspondientemente con su energía de centro de masa actual. Por lo tanto, se documenta la condición del detector, sus técnicas de adquisición y sus protocolos. Se hará énfasis en las Fibras de Centelleo (SciFi), uno de los futuros sub-detectores del LHCb, encargado del reconocimiento de patrones de trazas, basado en los cruces o impactos que ocurren sobre sus fibras. Además del registro de eventos significativos en la transmisión de datos. Este artículo presenta paso a paso las modificaciones aplicadas a los códigos para pasar del Modo Estándar al Modo de Bus Ampliado, incrementando la tasa de datos mediante la reducción de bits de control, para acrecentar el número de información analizable sobre los eventos.

Palabras clave: fibras centelleantes; detectores de partículas; LHCb; programación en VHDL; configuración de código.

INTRODUCTION

This article is part of the technological development and new findings in the field of high energy physics with application to data acquisition in the detection of elementary particles. These developments were implemented in collaboration with CERN about the experiments occurring in LHC, particularly with LHCb along with Universidad del Tolima, Universidad Nacional de Colombia and Universidad de Ibagué. The experiment took place in LPNHE (Laboratoire Physique Nucléaire et de Hautes Énergies) in Paris, France to assist in the development of programming codes for the optimization of data acquisition.

In order to take advantage of the planned modifications for the LHCb upgrade from 2018 to 2019 during the Long Shutdown 2 (LS2) for the improvement of its acquisition capacity and storage, the codes were managed for the event detection. The operation mode configurations for the acquisition boards to achieve higher efficiency using shorter sample times are presented here. The main feature of the LHCb upgrade will be an increase in the instantaneous luminosity of a factor of 5 compared to the current one, which is expected to improve the experiment's background, enhance the number of collisions and increase the accumulation of possible valid events [1-2]. This enhance the experiment in the pursuit of knowledge, as the statistics management of the data will be improved. It is to say that if the quantity of information is higher, then the mathematical treatment and its analysis will be more accurate. So the particles physics conclusions gathered at CERN claim to be supported by meaningful information.

There are several types of sub-detectors in LHCb. This paper will focus on Scintillating Fibers (SciFi) as one of the new intermediate layers of the future detection system. The SciFi is in charge of trace pattern recognition based on the hits received by this sub-detector and the recording of significant events in the transmission of data. The proximity of the detection layers to the beam-pipe determines their event density. This means that there has to be more than one operation mode because of the location of each Scintillating Fiber module, and

according to their occupancies [2-3]. Because of the above, an alternative operation mode is tested to check how it works, as an improvement of the standard one. This premise will be discussed shortly.

The code configurations were executed in VHDL programming language used in the experimental processes of CERN due to its low sampling times. This kind of language is useful because of the velocities, nearly the speed of light, operating at CERN. So, it is possible to collect more data, and if more data is collected the statistics issue discussed above will be easier to solve [4-5]. The experimental factor is decisive in scientific theory consolidation, which is the reason for specialized research centers in different areas. Consequently, this practice has to be done at CERN's laboratories with the LHCb collaboration [6-7-8-9-10].

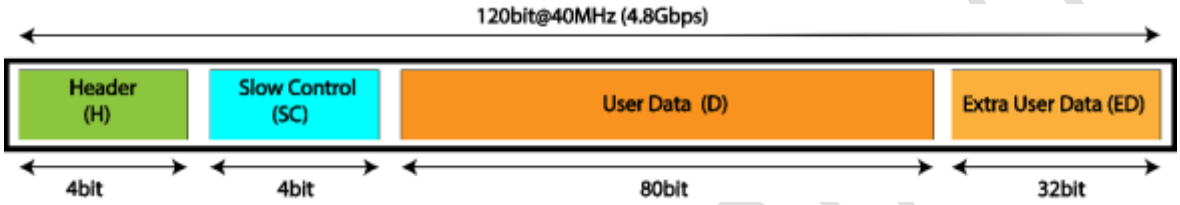

Fig. 1. Encoding frame.

Source: Adapted from CERN/LHCb, 2014 [11]

Two operation modes were studied in this experiment, which are Standard Mode and Wide Bus Mode. Each one has different useful features for the detection and recognition of events. The difference between them is the distribution of bits in the transmission and reception frame. The Standard Mode has a greater bit number of control and the Wide Bus Mode has a greater bit number of information about the events. The aforementioned modes have 120 bits per frame, distributed into four sections: Header (H - 4 bits), for the recognition of the first bits in a frame for the synchronicity and identification, Slow Control (SC – 4 bits), implemented in processes without significant times of recognition, User Data (D – depends on the use), for transmission of events and an Extra User Data (ED – depends on the use), as shown in Fig. 1 [11-12]. The ED could be implemented as a control scheme instead of increasing the User Data. Because of SEUs (Single Event Upset), the placement of the modes is defined by the radiation levels to which they are exposed.

The aim of the LHCb experiment is to study the CP violation regarding the decays that occur in flavor-changing particles based on the CKM matrix. These kinds of studies need data acquisition methods. Most of them are studied for B physics, where the probability of any event containing conclusions toward the matter-antimatter asymmetry is larger than with others, taking into account the less expensive operations [13-14-15]. There are different types of rare decay channels for the study of heavy-flavor physics, because of the transformation of B mesons into other particles. Their lifetimes are extremely short, so a vast sampling frequency is needed for the trace reconstruction [7-16-17-18-19]. It is recommended to have a lot of data to analyze the particle's behavior due to the more reliable statistics that plentiful data can yield. The sub-detectors are perpendicular to the incident beam-pipe, making the study of the electro-weak interactions, charge currents and QCD easier [6-7-18].

Due to the increase in luminosity in the LS2, an improvement in the acquisition data boards has to be done, not only in their hardware but in their inner codes. Currently, for RUN2, a luminosity of 8 fb^{-1} is expected, by adding up RUN1 and RUN2 results of 3 fb^{-1} and 5 fb^{-1}, respectively. This project is a part of the LHCb upgrade, where the integrated luminosity is expected to reach 50 fb^{-1}, with an instantaneous luminosity of $2x10^{33}cm^{-2}s^{-1}$ for the RUN3. If the luminosity is greater, then the probability of finding valid events is higher. In RUN2, the sampling frequency is 1MHz, but because of the luminosity increment, it is necessary to enhance the sampling frequency to over 40MHz. That is to say, one data frame every 25 ns, which will improve the decay channel range. This changes are important in the trigger system, due to the implementation times. It is to say that if the data acquisition velocity is higher, then a trigger management should be done to maintain a robust control of the events and their classification [1-3-20]. This matter will be discus in next chapter.

The document is divided into three chapters, which describe the procedure of the project. In the introduction it is expressed the purpose of the changes and the tools that have been taken into account for its consolidation. Chapter one, “Materials and methods”, is a study of the Scintillating Fiber sub-detector and the digital electronics that have been used, their operation modes and respective modifications. The second chapter, “Results and discussion”, is where the programming configurations are described in detail. The results are explained in an understandable way, so it is not mandatory to check the code itself. And finally, the conclusions, gather the hypothesis, background and results.

1. MATERIALS AND METHODS

The boards used in the transmission and reception were Stratix V GX, which are FPGAs equipped with high velocity optical fiber connections from Altera. The Stratix V GX is radiation efficient, which is why it is built as an ASIC [3-21-22]. To handle the new sampling frequency, the implementation of a new tracker in the intermediate stages of the detection is necessary, which introduces the SciFi to this upgrade. Furthermore, the intention of the SciFi will be to improve the acceptance of the detector. The SciFi is composed by Silicon Photo Multipliers (SiPM), built with 2.5 m fibers with a 250 µm diameter, arranged parallel so that when they are in contact with a particle trace or any event, they will generate an oscillating signal using a PLL for better definition and precision. The SiPM are found between the Readout Boxes on the top and bottom of the detector where the pixels are located [1-3-20-23-24-25]. All of the modifications in this project were made for this sub-detector. For this purpose, many protocols and sub-routines have been changed.

The signal trigger enhances and affords a higher quantity of data registration from the boards and storage resources. For that purpose, a Low Level Trigger (LLT) has been considered for implementation. This LLT determines the readout capacity and the utility of events for a better storage space in the buffers, by disregarding first-trigger decisions that do not seem to correspond to relevant data [3-20-26-27].

1.1 SCINTILLATING FIBERS

Considering the difficulties for big component transportation into the LHCb caverns, a modular division has to be made for the construction of the SciFi. This is built in

three stations with four layers per station, and each layer with four quadrants. Each quadrant is composed of 96 SiPM arrangements, with 128 channels per arrangement, for higher precision in the event location. The SiPM are solid-state devices for trace detection, which are considered active elements, due to the production of an optical oscillating signal [1]. The SiPM modules are built with two matrices of 64 silicon channels coupled in packages. Each pixel's size is 57.5μm×62.5μm, and since the channel has 96 pixels, its dimension is 0.25mm×1.5mm, depending on the pixel that is going to be implemented [1-28-29]. These SiPM arrangements are 2.5 m long, so they can be organized as a 5m×6m module for better acceptance. The SciFi characterization is defined by simulation processes and commercial photomultiplier implementation, in order to consider any advantages or disadvantages in the detection [23-24-30].

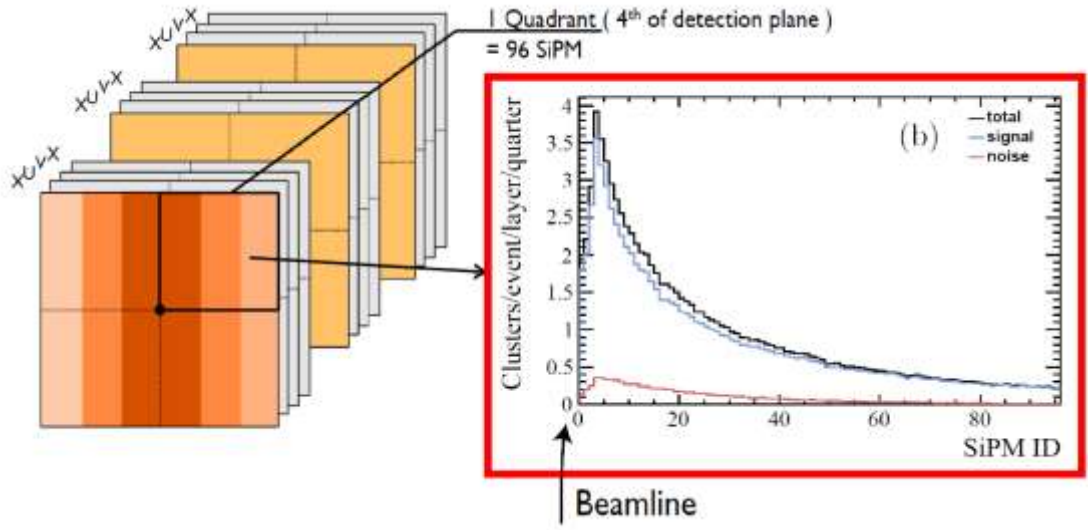

Fig. 2. Scintillating Fibers disposition with occupancy levels versus SiPM ID chart.

Source: Adapted from CERN/LHCb, 2014 [30]

As can be noted in Fig. 2, the noise corresponds to the after-pulse, one of the less desired, and more frequent signals in the background noise for the SiPM, due to the emission of a photoelectron. One of the most important mechanisms where these types of phenomena happen is in the ionization of residual gases, leading to the acceleration of a photoelectron within the photomultipliers. The back-scattered electrons also generate after-pulses in the dynodes (photomultiplier tube electrodes), which come back after traveling for a while inside the SiPM [30-31]. The SciFi layers are located equidistant to one another, inside the global system for a better resolution in the detection [1].

Each station is distributed into four detection layers whose given coordinate measures (X,U,V,X) for the SiPM are oriented as (0°,+5°,-5°,0°), with respect to the y axis for better precision in data acquisition. The first and last layers do not show any inclination, whereas those in-between are +5° and -5°, respectively. Their inclinations allow a more detailed observation of the actual points where the traces occur, by operating their intersections and comparing those results with the stations close to each channel.

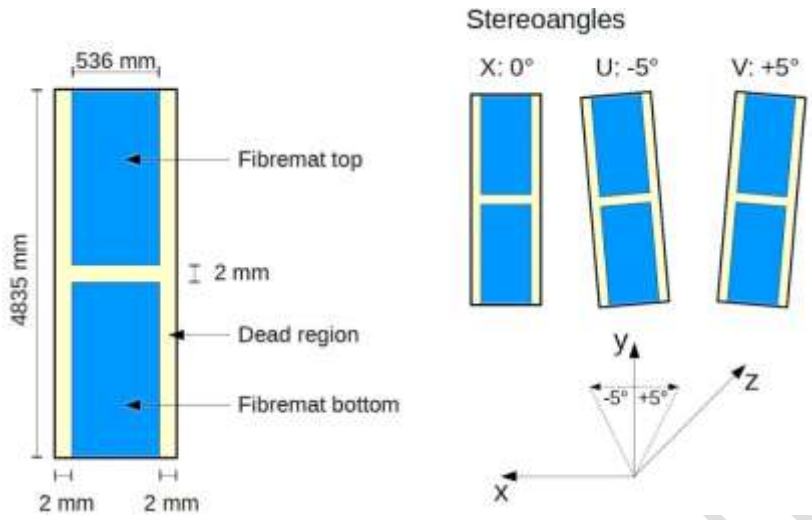

Fig. 3. The dimensions of a module, as described in the simulation and the definition of the stereo angles. The size of the dead material is increased to be visible.

Source: CERN/LHCb, 2014 [1]

The size of each sub-module of the SciFi is 540mm×4835mm, which are displayed in Fig. 3 [1-23]. The signal of one particle into the SciFi is typically registered by two or more detection channels, and a clusterization algorithm is necessary to combine the signals of those channels, because each pixel can detect only one photon. The collisions are detected in different layers of the experiment, each of them with a specific task in this complex endeavor. On average, there are 1.6 Bunch Crossings (BCX) per collision, even though it is expected to be between 3.8 and 7.6 BCX [6].

1.2 COMMUNICATION BETWEEN FE - BE THROUGH THE GBT

The data acquisition in CERN is gathered using VHDL because of its advantages in the sampling and efficiency for the code load. The Stratix V GX work under the name MiniDAQ, is assembled by structures known as AMC40. These boards are part of the three stages in the transmission and reception of the information in the LHCb cavern: Front End (FE), Back End (BE) and Gigabit Transceiver (GBT – Gigabit Bidirectional Trigger and Data Link) [32-33]. The codes in the final programming system could be written in different types of languages such as Verilog or C, but in the end, the final code is translated to VHDL. There are two centralization deposits, GIT and FORGE, which build the codes in collaboration with people around the world [12-34-35].

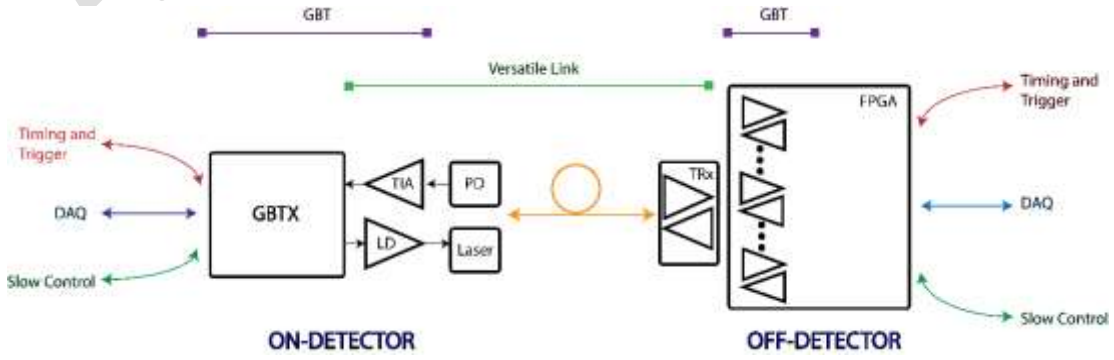

Fig. 4. Link architecture with the GBT chip set and the versatile link.

Source: Adapted from CERN/LHCb, 2015 [36]

There are two big parts of the detection in LHCb: On-detector and Off-detector, as shown in Fig. 4. The FE is located in the On-detector and represents the interface between the experiment and the data transmission. The Off-detector is located in the control rooms where the BE is situated. It is necessary to implement ASICs (Application Specific Integrated Circuit) in the experiment due to the SEUs in the On-detector region. ASIC devices have a higher robustness against radiation. For the BE, COTS (Commercial Off-The-Shelf) are used to reduce costs based on their location. Their connections are made through versatile links [36].

There are some blocks in the codes that have to be implemented for synchronization, trigger, data acquisition and slow control (SC). Some others are used in the coupling of modules, such as the TIA (Trans-Impedance Amplifier), PD (PIN Diode) and LD (Laser Driver) [36].

The control system works in the FE, BE and GBT due to the transmission and reception errors. The GBT requires control systems, such as Timing and Fast Control (TFC) and Experiment Control System (ECS), for the synchronization and organization of data before sending the frames. The most important processes for the signal transmission in 120 bit frames happen in the BE: de-codification, data alignment, BCX ID, LLT and the MEP (Multi Event Packet – construction of the packages). The LLT is useful for the collection and regulation of the buffers. There is a throttle that is in charge of moderating the data validity [37].

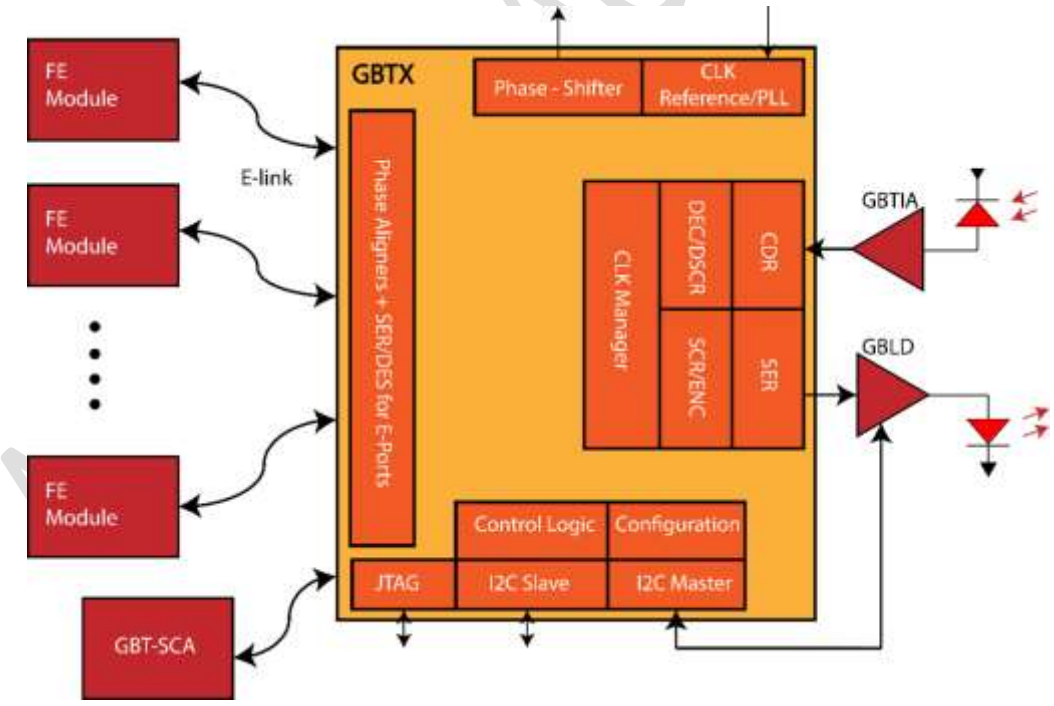

Fig. 5. GBT architecture and interfaces.

Source: Adapted from CERN/LHCb, 2015 [36]

The communication between FE and BE through GBT is made under a 10 Gigabit Ethernet. Two links are analyzed, the uplink (from FE to BE) and the downlink (from

BE to FE), these are shown in Fig. 5. The GBTIA for the downlink and the GBLD for the uplink serve as couplings. Some processes are made in-between these stages. In the uplink, the Scrambler/Encoder is implemented to achieve a DC balance. The Forward Error Correction (FEC) sends the signal into the Serializer for transmission through the GBLD. On the other hand, the downlink is made through the GBTIA for coupling with the Clock and Data Recovery (CDR) as high-speed serial information. There is a De-codification/Descrambler for tasks similar to the Scrambler/Decoder, but backwards. The downlink transmits the TFC+ECS protocols. Some versatile links are used in the interconnections of the FE with GBT and BE with GBT, using LVDS for the signal control [36].

The FEC is made by a Reed Solomon (RS) Encoder and Decoder with double-interleaving to deal with burst errors. It has a great control capacity, but it uses some bits of the frame in the control. This is a disadvantage, because 32 of the 120 bits are being used for something other than event information, reducing the amount of possible clusters in one frame, and making it less efficient. Nevertheless, the control represents security in the transmitted bits. The Scrambler uses a balancing system that takes random values with defined patterns from Boolean operations. This module is known as Scrambling Constants, used to ensure a proper distribution of 0's and 1's in the data flux. The Scrambling has to take place before the RS encoder, and the Descrambling after the RS decoder [36].

The GBT could be configured to be a bidirectional transceiver, or a unidirectional transmitter or receiver [38]. In terms of the LHCb upgrade, there is a new TFC, named Super TFC (S-TFC), which controls every state of the readout and the synchronization links, and is in charge of valid data control and throttle management. A Stand-Alone system allows the autonomous function of one or any group of sub-detectors, with a special mode of operation independent from the others, also known as partitioning [37].

For the communication between boards, a standard module has been designed under the name of Advanced Mezzanine Card 40 (AMC40). These structures are built to organize the external links and cabling for better control and synchronization in the readout. One AMC40 is composed of: Stratix V GX, configuration ports, a power supply, Ethernet communication, data acquisition ports for the GBT, clock circuitry and LED interfaces for the user. This configuration enables easier connections and standardizes the modeling system, so that the connections stay the same even when the operation configuration varies [12].

1.3 OPERATION MODES

The operation modes define the implementation processes of the data acquisition boards, so their configuration is of the utmost importance to this research. The current acquisition models and the required changes needed to improve the data collection were studied. Despite the fact that the boards have a similar hardware construction, they are configured depending on their occupancies. Each of these is made with transmission times of $25\,ns$ per frame, according to its sampling frequency of 40 MHz. The principal aim of this work is to suppress the large amount of control bits in the frame, so more information is sent through the User Data [36].

Fig. 6. GBT frame structure.

Source: Adapted from CERN/LHCb, 2015 [36]

The high data transfer control is a central feature of the Standard Mode, which can be a harmful, because the amount of bits used in control cannot be used in data transmission or clusters. Nonetheless, it is relevant due to the high radiation levels in the high occupancy regions of the detectors. The bit disposition of the frame is described in Fig. 6, organized as follows: 4 bits of Header, 4 bits of SC (divided into two parts, Internal Control (IC) and External Control (EC)), 80 bits of User Data (clusters and events), and finally, a 32 bit FEC. Thus, the efficiency is about $66.\bar{6}\%$ in each cycle, which corresponds to the ratio between the 80 bits of possible clusters and the total bit amount (80/120). The transmission bandwidth is 3.2 Gb/s, even though the bandwidth for the total frame is 4.8 Gb/s [36].

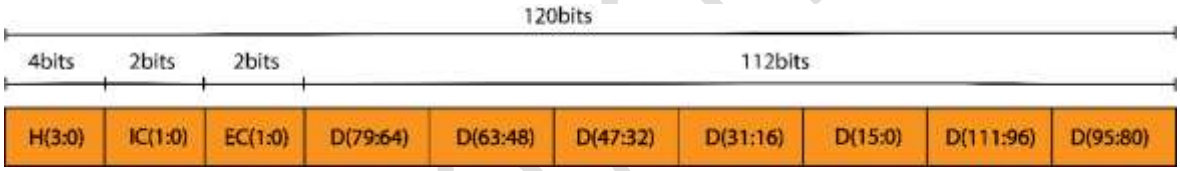

Fig. 7. Wide frame format on uplink.

Source: Adapted from CERN/LHCb, 2015 [36]

The Wide Bus Mode has a different distribution. The frame is organized as follows: the same 8 bits of control (Header and SC) and 112 bits of User Data. This change is relevant because its efficiency in data rate increases from $66,\bar{6}\%$ to over $93,\bar{3}\%$ due to the ratio between user data and the total frame bit number (112/120). Although its efficiency increases, the control decreases drastically. This distribution is shown in Fig. 7. The new efficiency allows the buffer to dispose of all of the idle data and enables the system to transmit a higher bandwidth of 4.48 Gb/s. With this modification, the code blocks vary notably. The Header has a data valid signal which is useful in the transmission and reception of the frame so that it can have precise processing. The signals must be DC balanced, which is one of the reasons why the Scrambling must be present whether there is FEC or not. Despite the fact that the Wide Bus Mode is being used for the uplink, the downlink still uses the Standard Mode format to send control to the caverns. When it comes to uplink, Wide Bus Mode is used for the transmission of the clusters from FE to BE, since there is not any need to send clusters through the downlink [36].

The Stratix V GX is capable of immediate simulation processes. In this respect, building data acquisition codes has the advantage of a preview analysis to fulfill the protocols of CERN. Test benches are proposed for simulation to estimate

hypotheses about how these systems would work under protocol conditions. The simulations are generated from a CCPC (Credit Card PC) with SC. These simulations are made by a Generic Data Generator, which sends information to the FE. This information is configured via a .txt document. Simulations are indispensable to avoid unnecessary execution outlay with the preview revision of the established formats. This configuration is made through a USB Blaster, so there is no need to disconnect the boards from the AMC40 to simulate, compile and program [36]. These boards can work as Stand-Alone for the simulation, configuration, control and operation of small-scale tests of the FE. The test benches must have emulated data to check the proper operation of the codes [12].

2. RESULTS AND DISCUSSION

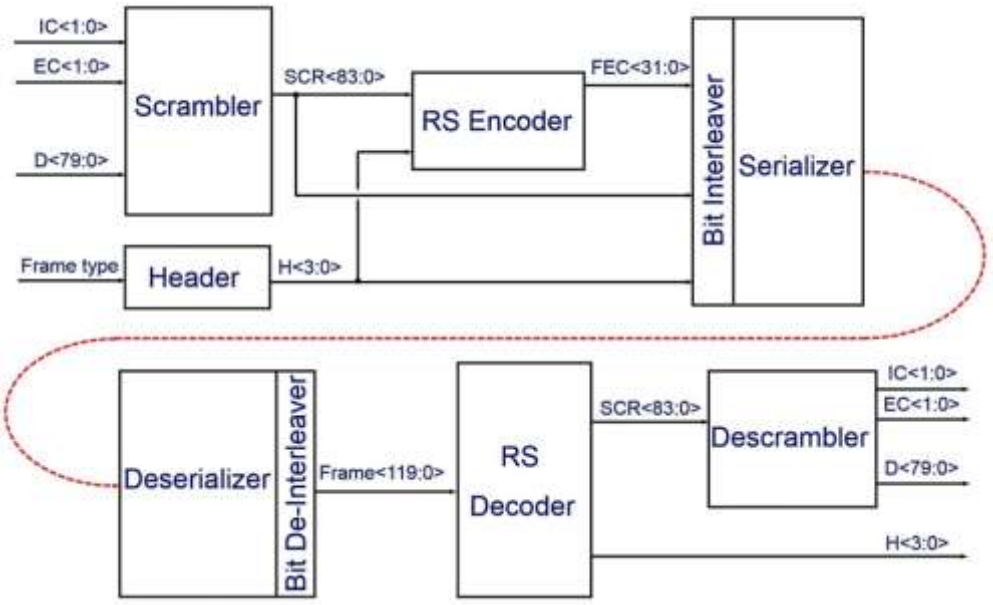

Fig. 8. Standard Mode GBT encoding and decoding block diagram.

Source: Adapted from CERN/LHCb, 2015 [36]

The following section will describe the configurations implemented in the corresponding modules for the data transfer. To improve understanding, one should refer to the block diagram of the two operation modes. The Standard Mode in Fig. 8 shows the blocks in the transmission stage on the top, and the reception stage below. Some of these modules were described before. The Bit Interleaver reorganizes the information for the serialization process before transmission. This information is transferred through the GBT link which is represented by the dotted line.

In the reception stage, the process is completely inverted as the information has to be de-serialized. The Bit De-Interleaver reorganizes the information for the RS decoder recognition. The frame enters the Descrambler to reset the signal as it was originally written into the transmission lines; according to the pattern constants, so that the clusters are arranged as they were first sent.

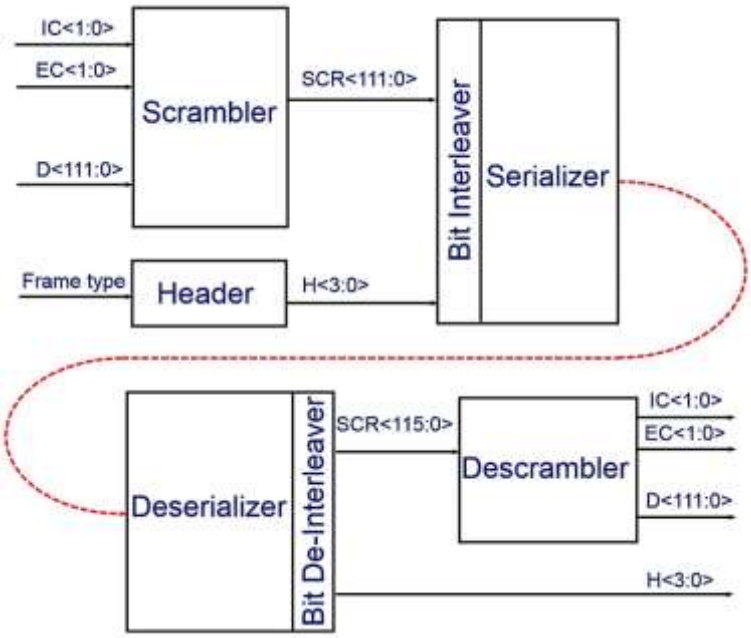

Fig. 9. Wide Bus Mode GBT encoding and decoding block diagram.

Source: Author, 2015.

Fig. 9 shows the Wide Bus Mode block diagram with the corresponding modifications. In essence, the changes are based on the quantity of bits for clusters and control. In the blocks inside this process some changes were done, and as a result, the RS Encoder and Decoder have to be cut out. For the GBT modification, each of its parts has to be studied. This preliminary stage requires the understanding and inspection of each module and subroutine which can be then implemented in the final program. Some of the modules are the product of firmware or templates in VHDL and Verilog, created by compilers such as the MegaWizard. To suppress the FEC control in the transmission is the principal aim of these configurations. The modifications are exposed from the most general program to the least, even though the changes were made the other way around.

2.1 CODE MODIFICATIONS

One condition that must be taken into account during the whole process is the number of bits modification in the inputs and outputs. The input word has to be changed from i_word(83:0) to i_word(115:0), considering the non-modification of the SC. These corrections were made in all the modules and sub-routines, starting with gbt_0 which is in charge of the initial values, constants and arguments.

2.1.1 General changes

Due to the size of the program, some sub-routines were used to divide the code into smaller blocks or packages. Inside these packages, some component declarations were made. Three of the fundamental packages are:

- Work.gbt_tx
- Work.multi_gigabit_transceivers
- Work.gbt_rx

These sub-codes are included as if they were libraries at the beginning of the top-level code. There are three of them: transmission, GBT and reception, one for each stage. Some other useful modules in the final code are declared as:

- Gbt_bank
- Vendor_specific_gbt_bank_package
- Gbt_banks_user_setup
- Gbt_bank_ID

These four refer to the GBT, the manufacturer characteristics, the adjustments to the program conditions and the package identification, respectively. In the Gbt_bank the data number is defined as follows: 84 for Standard Mode, and an extra number of bits are added for the Wide Bus Mode. The central code, Gbt_bank.vhd, is where the connections and parameters are declared, some of which are vendor-specific, in this case for Altera. The control ports are inside a GBT bank module classified into records in the <vendor>_<specific>_gbt_bank_package.vhd. There is a user-modifiable file, <vendor>_<specific>_gbt_bank_user_setup.vhd, where the adjustments take place to run with a specific board.

The user setup is in charge of simple input changes. It selects the operation mode and some other features. A MGT (Multi Gigabit Transceiver) is implemented inside the GBT, defined as a hard block. The MGT is in charge of serialization in transmission, and deserialization in reception. The GBT receptor aligns, decodes and descrambles the input signal.

In the construction of every code, sub-routine and module, several parameters have to be identified straight away. Two features for the modules are described and organized in the Gbt_bank_user_setup_R, which are configured through two constants as follows:

- 0 for GBT_FRAME or 1 for WIDE_BUS or 2 for GBT_8B_10B
- 0 for STANDARD or 1 for LATENCY_OPTIMIZED

These define the operation mode that will be implemented, as well as whether the latency optimization will be used or not. For latency optimization, the temporization resources become a critical factor, due to the high number of domains in the multi-link implementation of the clock.

2.1.2 Specific changes and port description

There are two significant modules for all of the codes: gbt_tx and gbt_rx, for transmission and reception, respectively. These are part of the code of the GBT, which are compiled over a top level. The modules will be described below.

- Transmission

The VHDL programming is aided by a block representation known as .BDF files (Block Design File) making input and output modifications of the code easier. There is an input for the transmission block which warns the program about events. The clocks have to be declared in 40 MHz and 120 MHz for the implementation of serializing and de-serializing. The bit quantity per port was changed. The input and output signals had to be changed for intermediate variables so that they would not

have any issue, and would not prejudice the functioning of the initialized vectors, such as “i” and “o”.

The GBT has a GearBox with multiplexor or demultiplexor (MUX/DEMUX) functions to prepare the signal for the MGT. The transmission block has a few sub-modules inside, the first of them is the Scrambling. It consists of a 40 MHz clock, data valid input, reset, 112 input for clusters and SC. In Standard Mode, the Scrambling is for 84 bits, therefore it has been divided into four scramblers with 21 bits each. For Wide Bus Mode, the groups must include 29 bits for each Scrambler so that a 116 bit Scrambling is constructed. Some scrambling patterns are selected at the beginning within the Scrambling_Constants to perform a bit interleaving inside this Scrambler code. That is to say, a sequence of bits allowing the transmission of a balanced DC frame with a simple coding or decoding scheme in the signal. The size of each Scrambling_Constants has been modified from Standard Mode to adjust the requirements of the Wide Bus Mode.

Inside the Scrambling blocks, several flip-flops are located with different writing and reading times for data storage. The Scrambling_Constants block only has one reset, four Reset_Pattern outputs, and a Header connected to a D flip-flop controlled by a 40 MHz clock. The Scrambling_Constants block defines the ports mentioned for the Scrambler_Reset_pattern implementation. The Header must be data valid so it enables the signals. There are four Scramblers configured in the same way, arranged to divide the information into four groups of 29 bits each. Some logic functions are added to fulfill the scrambling processes inside the Scrambling_Constants. At the end of the Scrambler, there are four Scrambled_word files that concatenate to make a 116 bit output. The outputs of the Scrambled_word and S_Header are connected with two flip-flips, one for data and the other for the synchronization of the header.

The second block in the gbt_tx for the Standard Mode is the Encoder. This one is not included in the Wide Bus format, due to its lower control operation. This RS Encoder has to be suppressed from the final code by not requiring a FEC. To know the functioning of this block allows its suppression, taking into account the fact that it is not a labor of simple omission. Inside the Encoder, there are two RS Encoder modules with the same structure of 44 bits each. They are split into two to become a double-error correction that consists of 4 bits each, and is what makes a 16 consecutive bit correction possible. Codified and non-codified outputs are declared with comparative purposes. Their internal processes are made instantiating a polynomial divider to apply the functions of the RS.

The next block is the Interleaver which has a *“for”* routine that interleaves the bits of the frame in order to encode the information and deliver it properly for the serialization. The Interleaver allows the RS to process its double-web control, and even if the RS is not implemented in the Wide Bus Mode, it should be kept in order to prepare the bits for the serial transfer.

The last module of the transmission stage is a MUX, which organizes packages of 120 bits to 40 bits in a higher transmission frequency. This is useful in the implementation of the MGT hard block for the serialization of the data. This MUX consists of two internal modules. The RW_TX_DP_RAM eases the organization of the signals of writing and reading for the MUX. Some intermediate signals are

defined for the writing and reading processes, without intervening with the definitive ones. This block is the one in charge of the organization of the bits in the MUX function, using a 40 MHz clock according to its original sampling time of 25 ns. After this, the 120 MHz clock is useful in the division of the frame into four. Three of the four sections are where the 120 bits are located. The fourth section is created keeping the programming logic in mind, where powers of 2 are necessary. Therefore, the last 40 bits are not read. Some counters inside the code are implemented to supervise the MUX addressing function.

The second module of the MUX is the TX_DP_RAM with an input of 160 bits. This block only reads the 120 MSB (Most Significant Bits). It is run through the MegaWizard and it defines the 120 and 40 MHz clocks. It is in charge of transmitting 40 parallel bits faster, in order to reach the same amount of information in the required 25 ns per frame. In the MUX and DEMUX, the MegaWizard is called upon to compile specific functions inside the FPGA blocks. After the MUX, the data is sent to the MGT hard block, which is in charge of the conversion of the 40 bit signal to serial.

- Reception

The second big module of the top level is the gbt_rx. In reception, as in transmission, similar processes occur with the input and output. Some intermediate variables are declared in order not to prejudice the initiation values during the logic operations of the code. Some event identification flags are created inside the code for data valid or idle, so three signals Data_valid, Start_of_packet and End_of_packet are declared. An output with the non-corrected data is used to compare with the corrected one in the reception process, in order to define whether the received data is correct or not. Or in any case, to define where the original data frame is needed. There is an input bit to check the alignment of the frame. The frame passes through the MGT hard block before the reception. It de-serializes the data and forms a 40 bit signal at 120 MHz, so that it reorganizes as it was first sent.

The first block inside the reception is the Manual Frame Alignment (MFA). All of the information goes inside the MFA in 40 bit packages through the RX_Parallel after passing through the MGT receptor. The Bit_Slip_Cmd moves the information in a serial line and is used to indicate where the Start_Bit should feed back the inputs to synchronize the frame. The synchronization is confirmed by the GX_Alignment_Done. This MFA consists of several sub-modules, starting with Modulo_40_Counter. It has a counter from 0 to 39 that organizes the 40 bit packages and revises the patterns in the Pattern_Search before they go into the DEMUX. Later in the process, there is a Write_RX_DP_RAM in charge of moving the information from left to right for the package building. Inside this block, the writing addresses are generated for the reception. Here, something similar to the organization that takes place in the MUX happens, but in reverse, where the bits are organized into groups of 40 by shifting the original signal. After this process, the signal goes into the Pattern_Search and the DEMUX.

The pattern search does not have sub-modules, so it is a little bit longer and complex. This module checks the Header in the frame 4 MSB. First, it verifies whether it is data valid or idle. Some constants have to be declared at the beginning

so as to compare with the incoming frame, just for control issues. This is useful in the recognition of the amount of incoming clusters.

To ensure the robustness of the synchronization, there is a frame lock and a frame tracking routine. During the frame lock, the receptor must be blocked in the least amount of time possible, in order to minimize the death time in case there are losses during the normal operation. In the frame tracking, the receiver must avoid the reset of the block cycle unless there are plenty of consecutive errors, so that the buffers do not get overcharged.

The next module is the DEMUX that is in charge of the opposite task of the MUX, which has modules inside of it. The first one is the Read_RX_DP_RAM, which detects the value of the Write_address, confirming that the first data valid was written, and then starts reading the signal. Another intermediate block named RX_DP_RAM works under the management of the MegaWizard, where the information is reorganized to be sent through a 120 bit parallel port.

The next block is the reverse_interleaving, which is in charge of the inverse function of the interleaver. It accommodates the signal without following clock cycles. Because the decoding is just for Standard Mode, it is not implemented in this research. Therefore, the same conditions that were taken into account for the encoding stage were also applied to the decoding. The next module is the Descrambling, which has 4 sub-modules divided into 29 bit groups, just as the Scrambling has, but doing the inverse operation. It reorganizes the information and receives it properly. Similar to the Scrambler, the pattern correspondence is made between the input signals for the DC balancing by several Boolean operations. An adaptation from a Verilog code has to be done in this case. The Boolean operations in the Descrambler are very similar to the Scrambler ones. When the four sub-modules are outputted, a concatenation of one parallel output has to be done for a large Descrambling that includes all the data.

The last block in the reception stage is responsible for confirming the alignment of the data with a Start/End Packet, defined at the beginning and at the end of the packets to be read at 40 MHz. All these changes were made for the configuration of the operation modes to reach higher data transmission efficiency. The inner codes have fulfilled the requirements for the simulations, and the formats were proven to function under CERN protocols.

3. CONCLUSIONS

The scintillating fibers are the principal mechanism in the development of this article. Furthermore, the modifications exposed are applied to the data acquisition boards in order to improve the event analyses, and the increase in data makes it possible to apply the corresponding statistics. The resolution level will be enlarged because of the improvements that have already been applied, and the ones that will take place during the LS2. In the study of elementary particles, the construction of these fibers and their data recuperation methods will help the recognition processes.

The modifications of the GBT code between the FE and BE represents an improvement in the efficiency of cluster transmission. The operation modes configuration from Standard Mode to Wide Bus Mode took place in the VHDL routine implementation, establishing a data recollection system for the regions further from

the beam-pipe, also known as low occupancy regions, which represent almost 80% of the acceptance of the experiment. The application of the Wide Bus Mode is not justified in the high occupancy regions, due to the high radiation levels presented. Because of the bigger amount of SEUs in the data acquisition, it is inevitable to use a control as a part of the frame. Therefore, the Standard Mode is needed in high occupancy regions due to its FEC.

The implementation of this operation mode is highly important for the data acquisition, due to the amount of data needed to generate conclusions for high energy physics through the statistical processes involved. The high data rate with this new mode recognizes that the storage capacity may suffer significant consequences in the usage of the data valid and idle inside the codes. The data valid flag allows only useful data storage by ignoring the idle ones. The buffers may dispose of unnecessary information thanks to the application of these programming sub-routines, which permits the data transmission efficiency to increase from about 66.6% to 93.3% of the frame.

The implementation of VHDL in the acquisition processes of CERN is due to its hardware-oriented programming that makes a more efficient reception and transmission possible because of its high sampling frequencies. This tool is fundamental in the development of the LHCb upgrade in order to achieve a higher robustness.

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