An 8-bit TDC implemented with two nested Johnson counters

Un TDC de 8 bits implementado con dos contadores Johnson anidados

Jonathan Santiago-Fernandez[1], Alejandro Diaz-Sanchez[2], Gregorio Zamora-Mejia[3], Jose Miguel Rocha-Perez[4]

Santiago-Fernandez, J; Diaz-Sanchez, A; Zamora-Mejia, G; Rocha-Perez, J. M. An 8-bit TDC implemented with two nested Johnson counters. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 79-87.

https://doi.org/10.18845/tm.v36i6.6769

1 Instituto Nacional de Astrofísica, Óptica y Electrónica, México.
Email: sfernandez@inaoep.mx
https://orcid.org/0000-0002-3515-331X
2 Instituto Nacional de Astrofísica, Óptica y Electrónica, México.
Email: adiazsan@inaoep.mx
https://orcid.org/0000-0003-4529-6864
3 Instituto Nacional de Astrofísica, Óptica y Electrónica, México.
Email: gregorio.zamora@inaoep.mx
https://orcid.org/0000-0002-6509-0305
4 Instituto Nacional de Astrofísica, Óptica y Electrónica, México.
Email: jmiguel@inaoep.mx
https://orcid.org/0000-0002-3694-2468

Keywords

TDC; Jonhson counter; semi-dynamic logic; nested counters; time-lapse measurement; time-to-digital converter.

Abstract

This work presents a Time-to-Digital Converter implemented using two nested Johnson counters and suitable for time-lapse measurement applications. The proposed structure is composed of two 4-bit nested counters, two digital-logic control networks, two registers and a single decoder. Semi-dynamic logic was used for the decoder to reduce its power consumption. The system has a standard digital output and is powered by a 1.8 V supply with a total power consumption of 32.4 mW. A prototype was fabricated using a TSMC 180 nm CMOS technology. The proposed structure uses a 508 µm x 225 µm area. In addition, this TDC has a standard deviation of 0.78 LSB with a fixed input time interval operating at a frequency of 1 MHz. The proposed structure shows good performance results and repeatability for continuous conversion conditions, these results are attributed to the simplicity of the system and the use of counters with minimum gate delay as the main elements for the TDC.

Palabras clave

TDC; contador Johnson; lógica semi-dinámica; contadores anidados; mediciones de intervalo de tiempo; convertidor de tiempo a digital.

Resumen

Este trabajo presenta un Convertidor de Tiempo a Digital implementado utilizando dos contadores Johnson anidados y apropiado para aplicaciones de medición de intervalo de tiempo. La estructura propuesta se compone de dos contadores anidados de 4 bits, dos redes de control lógico-digital, dos registros y un decodificador. Para el decodificador se ha utilizado una lógica semi-dinámica para reducir su consumo de energía. El sistema tiene una salida digital estándar y se alimenta con una fuente de 1.8 V con un consumo total de 32.4 mW. Se fabricó un prototipo utilizando una tecnología CMOS de 180 nm de TSMC. La estructura propuesta ocupa un área de 508 µm x 225 µm. Además, este TDC tiene una desviación estándar de 0.78 LSB con un intervalo de tiempo de entrada fijo que opera a una frecuencia de 1 MHz. La estructura propuesta muestra buenos resultados de rendimiento y repetibilidad para condiciones de conversión continua, estos resultados son atribuidos a la simplicidad del sistema y al uso de contadores con mínimo retardo de puerta como elementos principales para el TDC.

Introduction

The channel length reduction and node scalling of CMOS technologies has greatly benefited the areas of digital design, digital signal processing, and the design of processor architectures, allowing the development and implementation of increasingly complex digital systems and algorithms [1]. Because current digital systems have high switching speeds, the timing resolution of digital circuits has greatly excelled compared to the voltage resolution of analog circuits implemented on CMOS scales of nanometer technologies [2]. This leads to a new approach to signal processing: Time-Mode Signal processing (TMSP).

The arrangement for TI evaluation is shown in Figure 1, where a time instant is measured between the changing edges of two voltage pulses connected to the *Start* and *Stop* inputs of the Time Interval Meter (TIM) [3]. This two pulses can be developed by comparators or discriminators,

which are handled in order to obtain information from signals coming from sensors or detectors of various temporal events, such as radiation flashes in systems using Positron Emission Tomography (PET) [4] and Single Photon Emission Computed Tomography (SPECT) [5]. TIMs execute the count of a time-lapse τ into a binary word. Therefore, a TIM is also called a Time-to-Digital converter (TDC). A TDC is liable for turning a time interval between two clock signals into a digital character.

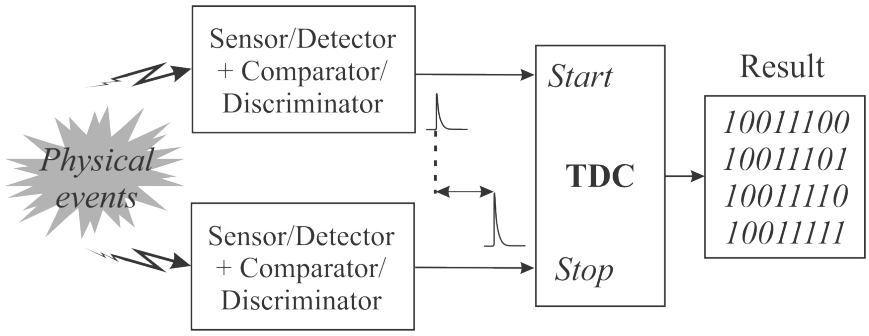

Figure 1. Principle of time-lapse measurement.

In this work, we propose a TDC structure that is composed of two nested counters. The remainder of this paper proceeds as follows. First, Section II describes in detail how the presented structure is composed, as well as a brief description of the operation of its blocks. Then, the experimental results are presented in section III and in the last part, section IV the conclusions of this work are discussed.

Proposed structure

The block diagram of proposed structure is ilustred in Figure 2, which is an 8-bit TDC, the system made up of two nested 4-bit counters, two logic-digital control networks, two registers and a decoder. This proposal has the advantage of having a great integration capacity and high resolution and range. The TDC operating mechanism proposed is as follows. The digital logic blocks are in charge of handling external signals to the converter to obtain the clock signals *CLK* and *CLK1*, for counters 1 and 2 correspondingly.

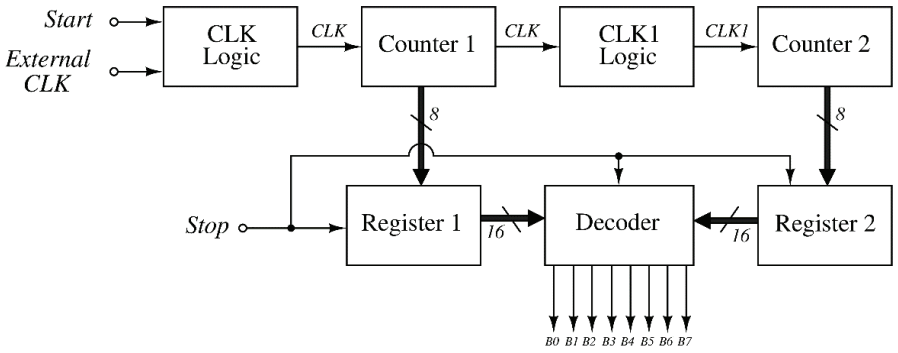

Figure 2. Block diagram of the proposed 8-bit TDC.

The counter blocks are in charge of measuring the time interval between the *Start* and *Stop* pulses. Likewise, the two registers blocks save the state in which the counters stay when the *Stop* pulse occurs. Finally, the binary word stored in each register enters to a decoder that is responsible for delivering a standard 8-bit word to the output of the converter. The implementation

of the counters where based on Johnson type (ring) structure [5], the above is due to the fact that our counter is intended to have a minimum gate delay. Johnson type counters have the characteristic that in each count only one element is activated, that is, there would only be a minimum gate delay between counter events.

The decoder block was proposed under a semi-dynamic logic [6]. The set (1) shows the logic functions used for the 8-bit output of the decoders, where the functions of the bits *B1* to *B4* are obtained by logic values that go from Q_1 to Q_8, which are the outputs corresponding to register 1. Functions of the bits *B5* to *B8* are similar to the previous ones, except that now the values given by register 2 are used. The type of logic used in this work allows decoding with lower power consumption.

$$B1 = Q_8 \cdot \overline{Q_7} + \overline{Q_8} \cdot Q_7 + Q_6 \cdot \overline{Q_5} + \overline{Q_6} \cdot Q_5 + Q_4 \cdot \overline{Q_3} + \overline{Q_4} \cdot Q_3 + Q_2 \cdot \overline{Q_1} + \overline{Q_2} \cdot Q_1 \quad (1a)$$

$$B2 = Q_5 \cdot Q_4 \cdot \overline{Q_7} + \overline{Q_5} \cdot \overline{Q_4} \cdot Q_7 + Q_3 \cdot \overline{Q_1} + \overline{Q_3} \cdot Q_1 \quad (1b)$$

$$B3 = Q_8 \cdot Q_5 \cdot \overline{Q_1} + \overline{Q_8} \cdot \overline{Q_5} \cdot Q_1 \quad (1c)$$

$$B4 = Q_1 \quad (1d)$$

Experimental results

After designing the proposed structure, the layout of the TDC was made using TSMC 180 nm CMOS technology. The developed prototype uses an area of 508 µm x 225 µm and is composed of two 4-bit nested counters, two digital-logic control networks, two registers and a decoder. A microphotography of the TDC that was elaborated can be observed in Figure 3. The circuit has an 8-bits digital output and is powered with a supply of 1.8 V with a total power consumption of 32.4 mW.

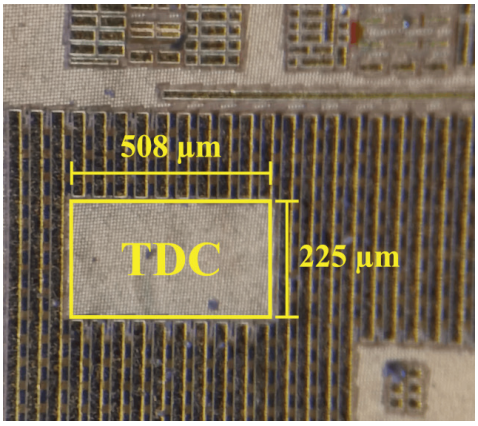

Figure 3. Microphotography of the proposed TDC.

The first test to be performed was to verify the behavior of the system in general; this was done by verifying the performance of the control logic responsible for generating the *CLK* and *CLK1* signals. The test was performed by connecting the device under test to the *Keithley programmable 3-channel DC power supply 2230-30-1*, the power supply voltage for the circuit

is 1.8 V. Additionally, a *WaveStation 3162 Teledyne LeCroy 2-channel Function Generator* was used by selecting a 1.8 V amplitude square wave output with a frequency of 1 MHz and a dutty cycle of 50%, this signal was connected to the *External CLK* input of the system.

In addition to the input signal described above, the *Start* signal of the system was enabled at a fixed value of 1.8 V, this in order to display the signals of interest for this test. The signals were visualized using a *Tektronix Digital Oscilloscope DPO7104*, in the Figure 4 shows the results of this test. The *CLK1* signal is produced every 16 events of the *CLK* signal, which serves to control the events of the two counters. Corroborating the function of these two signals we can make sure that the innards of the system is working properly.

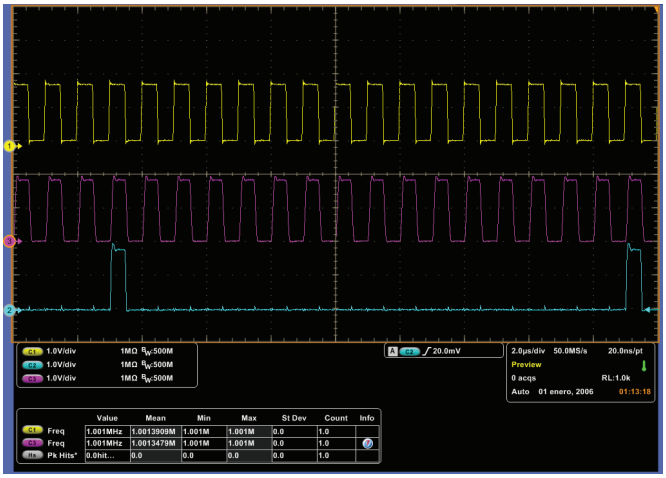

Figure 4. External clock signal and internal clock signals CKL and CLK1 of the proposed TDC.

The next test performed to the proposed TDC is to obtain all the count codes for the 8-bit output. To perform this measurement, two out of phase clock signals were used for the *External CLK* and *Start* inputs, the frequency, amplitude and dutty cycle of the signals is the same as in the previous test. To obtain the results of this test, a *Keysight 16851A 34-Channel Logic Analyzer* was used, which were configured to get the logic states of the output bus and the signals of interest to be measured.

The results of this measurement are presented in Figure 5, where part of the output codes obtained can be observed, being these from code 114 to 120. Subsequently, in Figure 6 a graph with the characteristic curve is observed, which contains all the output codes for the complete conversion range of the TDC, it should be noted that an approach to the graph was made in the same interval as the capture made to the logic analyzer.

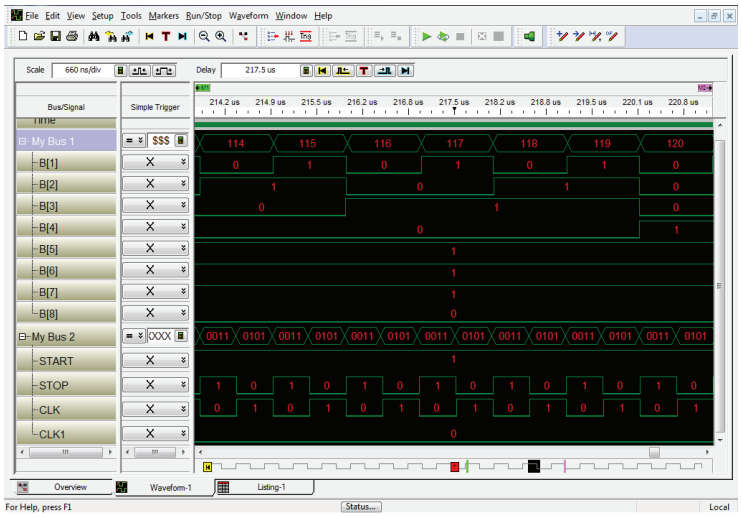

Figure 5. Screenshot of the TDC characteristic curve measurement.

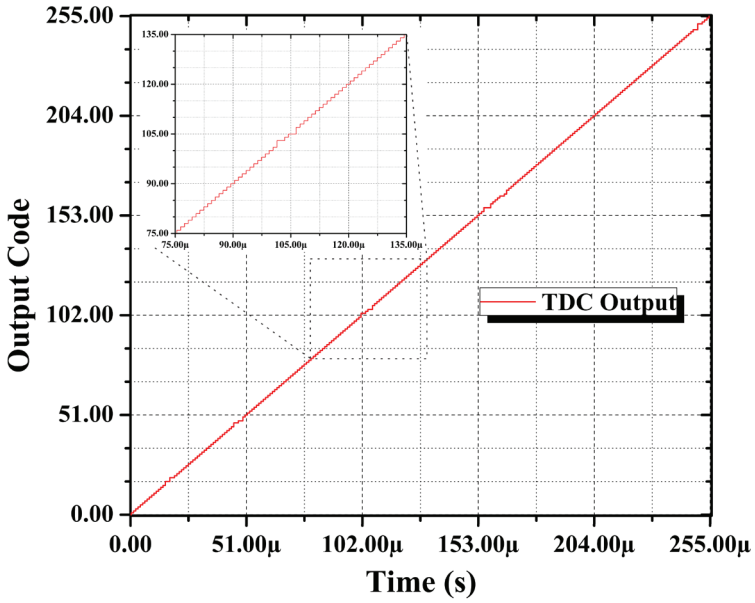

Figure 6. Characteristic curve of the proposed TDC.

Finally, a single-shot test was performed by configuring the TDC input time interval to keep it fixed during the measurement; the purpose of this is to obtain the standard deviation (σ) of the output distribution. The test was performed by taking 1000 samples of a fixed conversion interval with an output code of 117. The results of the single-shot test are shown in Figure 7, the standard deviation obtained was 0.78 LSB for this input conversion interval.

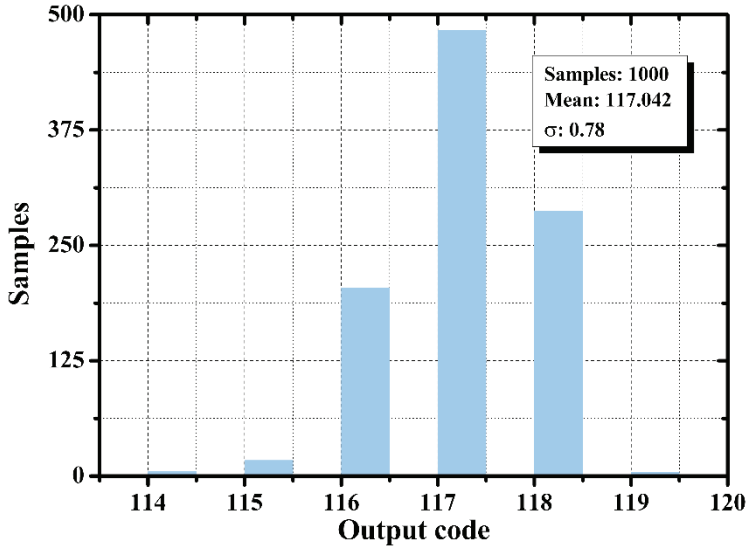

Figure 7. Test result the single-shot code distribution of the proposed TDC.

The proposed structure shows good performance results and repeatability for continuous conversion conditions, these results are attributed to the simplicity of the system and the use of counters with minimum gate delay as the main elements for the TDC, the tests performed affirm that it is possible to develop simple structures with outstanding performance using mature 180 nm technology.

Summary and conclusions

One of the many favorable consequences of technological scaling is that the time resolution of digital circuits has surpassed the voltage resolution of its analog counterpart. TDC's are widely used system to perform time-mode processing because they are easy to implement due to their simple structures and the diverse variety of applications they have. Along with the structure presented hereunder we intend not pursue an ordinary delay line configuration. With this configuration that makes use of two nested counters, good repeatability results can be obtained and although in certain cases output code errors do occur, these can be minimized by using layout techniques such as the implementation of ground planes, as well as increasing the operating frequency by using special high-speed output pads, thus improving the time resolution which is a very important feature of TDS's.

Time-mode signal processing arises as a response to the need to study new physical phenomena that occur with such small magnitudes and at such high speeds that were previously considered non-existent. Therefore, the study of time-to-digital converters offers a wide area of opportunity for the development of various fields of research and technological advances in the future.

Acknowledgment

The authors would like to thank the National Council of Science and Technology, Mexico (CONACyT) for the for the doctoral grant A1-S-43214. We also thank the National Institute of Astrophysics, Optics and Electronics (INAOE) for the technical training and for providing the use of their laboratories and equipment. And last but not least, we thank the R9 EDS ASIC Design Fabrication contest organizing and judging committee for choosing our design as the winner.

References

[1] Moore, Gordon E. “No exponential is forever: but “Forever” can be delayed![semiconductor industry].” In 2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC., pp. 20-23. IEEE, 2003.

[2] Staszewski, Robert Bogdan, Khurram Muhammad, Dirk Leipold, Chih-Ming Hung, Yo-Chuol Ho, John L. Wallberg, Chan Fernando et al. “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS.” IEEE Journal of Solid-State Circuits 39, no. 12 (2004): 2278-2291.

[3] Porat, Dan I. “Review of sub-nanosecond time-interval measurements.” IEEE Transactions on Nuclear Science 20, no. 5 (1973): 36-51.

[4] Mandai, Shingo, Vishwas Jain, and Edoardo Charbon. “A $780 X 800 μm^2 Multichannel Digital Silicon Photomultiplier With Column-Parallel Time-to-Digital Converter and Basic Characterization.” IEEE Transactions on Nuclear Science 61, no. 1 (2014): 44-52.

[5] Faramarzpour, Naser, M. Jamal Deen, Shahram Shirani, and Qiyin Fang. “Fully integrated single photon avalanche diode detector in standard CMOS 0.18-μm Technology.” IEEE Transactions on electron devices 55, no. 3 (2008): 760-767.

[6] Rai, Abhishek, and Rajesh Mehra. “Optimized Design and Simulation of 4-Bit Johnson Ring Counter Using 90nm Technology.” International Journal of Research in Advent Technology 16, no. 6 (2018): 1002-1006.

[7] Kumar, Sandeep, M. K. Suman, and K. L. Baishnab. “A novel approach to thermometer-to-binary encoder of flash ADCs-bubble error correction circuit.” In 2014 2nd International Conference on Devices, Circuits and Systems (ICDCS), pp. 1-6. IEEE, 2014.

LAEDC 2022 LATIN AMERICAN ELECTRON DEVICES CONFERENCE

An 8-bit TDC implemented with two nested Johnson counters

1st Jonathan Santiago-Fernández
Departamento de electrónica
Instituto Nacional de Astrofísica, Óptica y Electrónica
Puebla, México
sfernandez@inaoep.mx

2nd Alejandro Díaz-Sánchez
Departamento de electrónica
Instituto Nacional de Astrofísica, Óptica y Electrónica
Puebla, México
adiazsan@inaoep.mx

3rd Gregorio Zamora-Mejía
Departamento de electrónica
Instituto Nacional de Astrofísica, Óptica y Electrónica
Puebla, México
gregorio.zamora@inaoep.mx

4th José Miguel Rocha-Pérez
Departamento de electrónica
Instituto Nacional de Astrofísica, Óptica y Electrónica
Puebla, México
jmiguel@inaoep.mx

I. Introduction

THE channel length reduction and node scalling of CMOS technologies has greatly benefited the areas of digital design, digital signal processing, and the design of processor architectures, allowing the development and implementation of increasingly complex digital systems and algorithms. The arrangement for TI evaluation is shown in Fig. 1, where a time instant is measured between the changing edges of two voltage pulses connected to the *Start* and *Stop* inputs of the Time Interval Meter (TIM). TIMs execute the count of a time-lapse τ into a binary word. Therefore, a TIM is also called a Time-to-Digital converter (TDC). A TDC is liable for turning a time interval between two clock signals into a digital character.

In this work we propose a TDC structure which is composed of two nested counters. The remainder of this paper proceeds as follows. First, section II describes in detail how the presented structure is composed, as well as a brief description of the operation of its blocks. Then, the experimental results are presented in section III and in the last part, section IV the conclusions of this work are discussed.

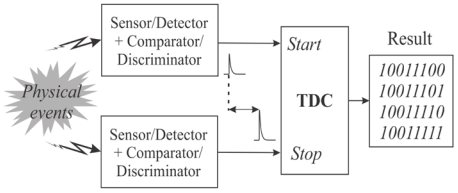

Fig. 1. Principle of time-lapse measurement.

II. Proposed Structure

The block diagram of proposed structure is ilustred in Fig. 2, which is an 8-bit TDC, the system made up of two nested 4-bit counters, two logic-digital control networks, two registers and a decoder. The digital logic blocks are in charge of handling external signals to the converter to obtain the clock signals *CLK* and *CLK1*, for counters 1 and 2 correspondingly.

The implementation of the counters where based on Johnson type (ring) structure, the above is due to the fact that our counter is intended to have a minimum gate delay. The decoder block was proposed under a semi-dynamic logic. The type of logic used in this work allows decoding with lower power consumption.

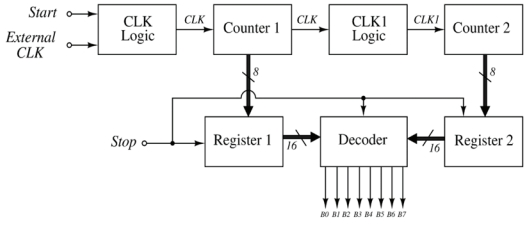

Fig. 2. Block diagram of the proposed 8-bit TDC.

III. Experimental Results

After designing the proposed structure, the layout of the TDC was made using TSMC 180 *nm* CMOS technology. The developed prototype uses an area of 508 *µm* x 225 *µm* and is composed of two 4-bit nested counters, two digital-logic control networks, two registers and a decoder. A microphotography of the TDC that was elaborated can be observed in Fig. 3. The circuit has an 8-bits digital output and is powered with a supply of 1.8 *V* with a total power consumption of 32.4 *mW*.

The next test performed to the proposed TDC is to obtain all the count codes for the 8-bit output. The results of this measurement are presented in Fig. 4, in which a graph with the characteristic curve is observed, which contains all the output codes for the complete conversion range of the TDC.

Finally, a single-shot test was performed by configuring the TDC input time interval to keep it fixed during the measurement, the purpose of this is to obtain the standard deviation σ of the output distribution. The results of the single-shot test are shown in Fig. 5, the standard deviation obtained was 0.78 *LSB* for this input conversion interval.

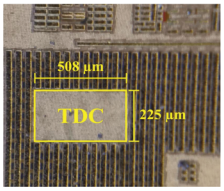

Fig. 3. Microphotography of the proposed TDC.

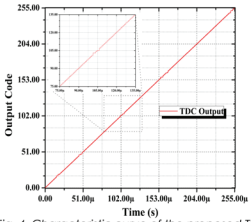

Fig. 4. Characteristic curve of the proposed TDC.

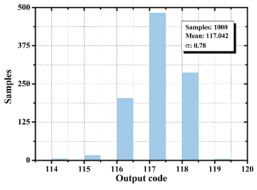

Fig. 5. Test result the single-shot code distribution of the proposed TDC.

IV. Conclusions

The proposed structure shows good performance results and repeatability for continuous conversion conditions, these results are attributed to the simplicity of the system and the use of counters with minimum gate delay as the main elements for the TDC, the tests performed affirm that it is possible to develop simple structures with outstanding performance using mature 0.18 µm technology.

Time-mode signal processing arises as a response to the need to study new physical phenomena that occur with such small magnitudes and at such high speeds that were previously considered non-existent. Therefore, the study of time-to-digital converters offers a wide area of opportunity for the development of various fields of research and technological advances in the future.

IEEE Advancing Technology for Humanity
2022 IEEE Latin American Electron Devices Conference (LAEDC)
Electron Devices Society

Illustration 1. Presented Poster at LAEDC 2022.